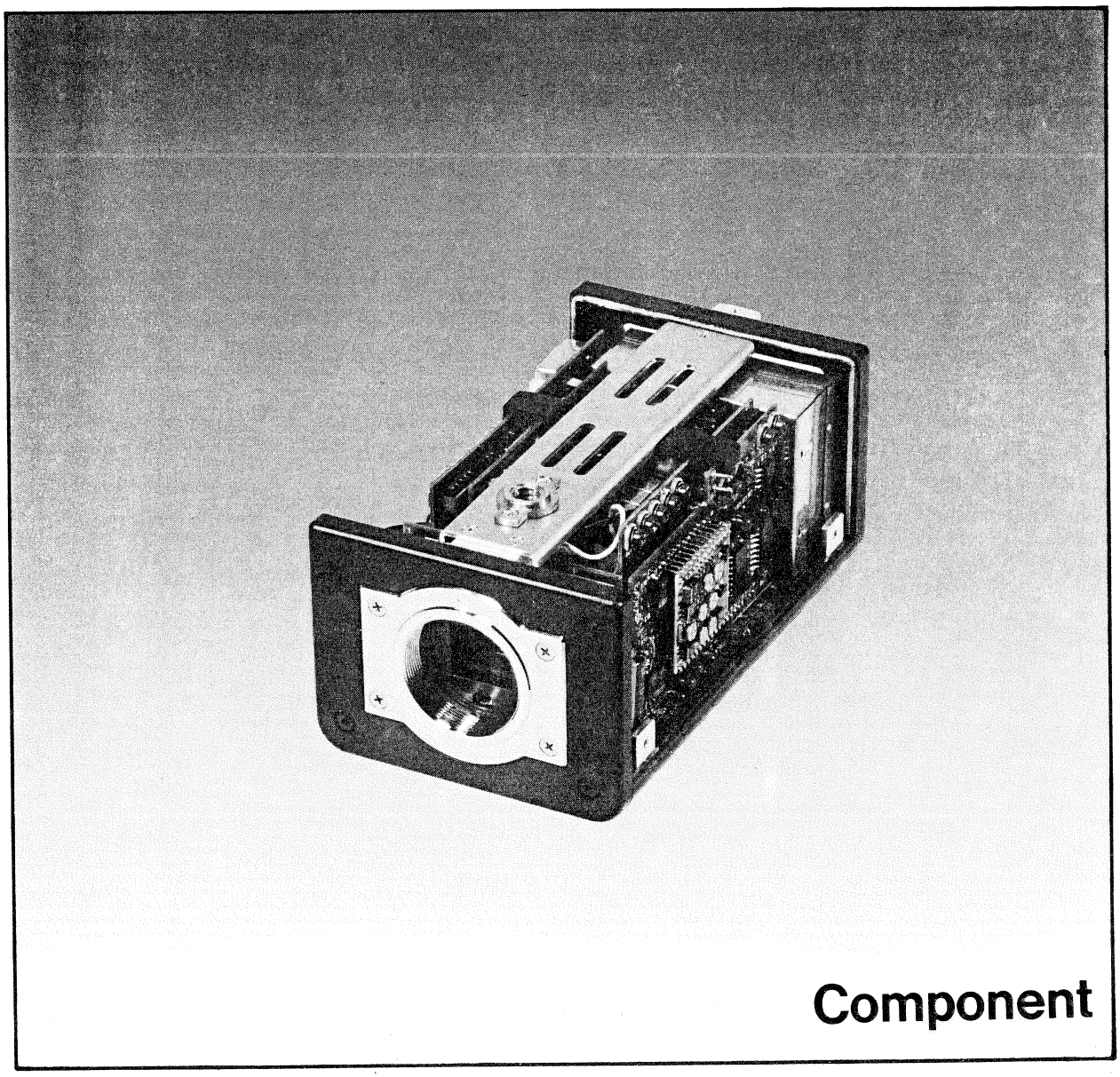
SONY

CCD

COLOR
Video Camera Module

XC-117/117P

THEORY OF OPERATION



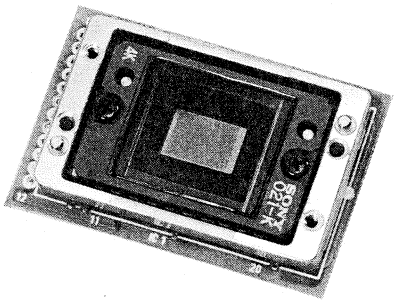
Component

PICK-UP DEVICE

CCD Chip

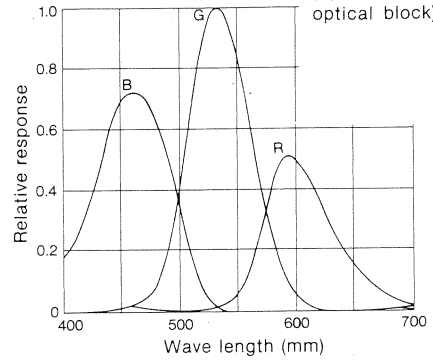
ICX-018K (NTSC)

ICX-021K (PAL)



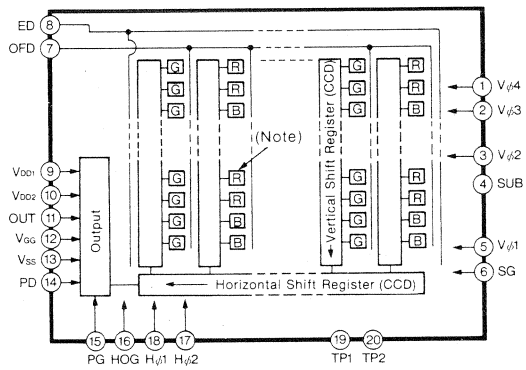
Spectral Response

(Specification with optical block)



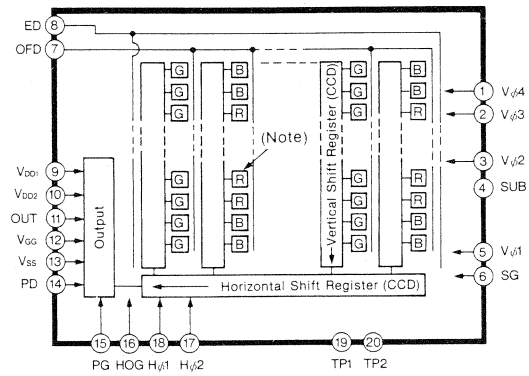
CCD Block Diagram
(CCD photo sensors location)

NTSC



(Note) -□- : Photo senser

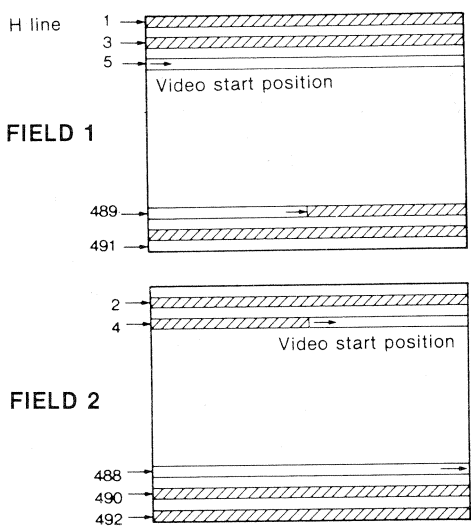
PAL



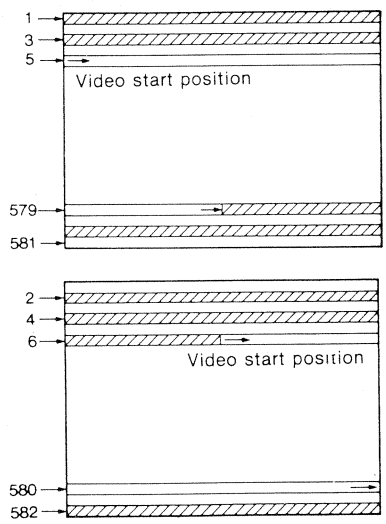
(Note) -□- : Photo senser

(V SCANNING)

NTSC

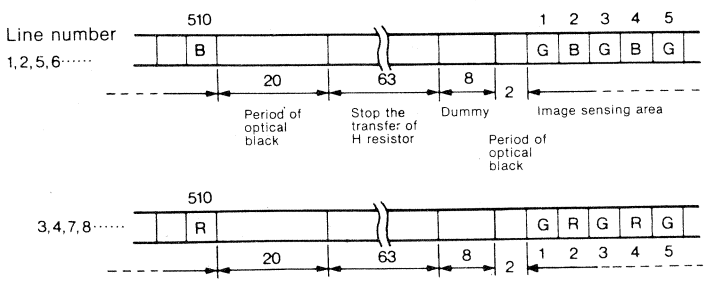


PAL

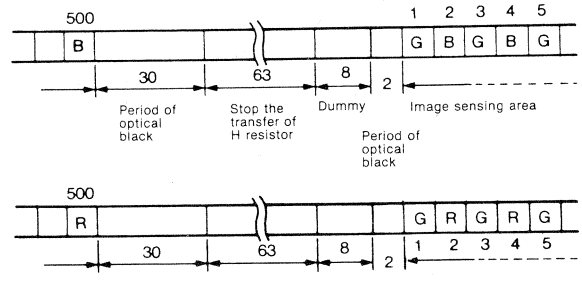


(H SCANNING)

NTSC



PAL



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1. BASIC PRINCIPLES OF CCD

. CCD

A CCD is a semiconductor storage device containing regularly arranged MOS capacitors. It processes electrons (electric charges) in the following sequence:

(1) Photoelectric conversion (An electric charge is generated using light.)

(2) Charge storage (An electric charge is stored.)

(3) Transfer/time operation (An electric charge is transferred.)

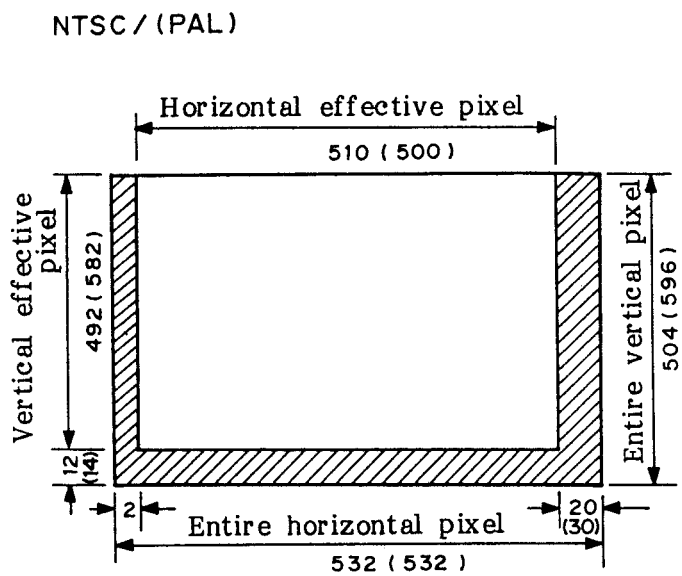


Fig. 1-1 CCD Imager ICX-018 (NTSC)/ICX-021 (PAL)

. Imaging system

When a solid-state image sensor such as a CCD is used for a color video camera, a very large number of pixels is required to obtain high picture quality. Since the effective number of pixels is limited to 510(H) x 492(V) = 250,920, an imaging system which reduces the number of pixels is required to prevent picture quality deterioration.

For PAL systems, the number of pixels is (H) x (V) = .

As shown in Fig. 1-2, this system employs an interline transfer system using a color filter.

RGB must be repeated for the conventional system. For the interline transfer system, however, RGB is repeated at a 2-pixel pitch using a horizontal color filter. The resultant 3/2 times sampling frequency enables higher resolution.

Moreover, one pixel which is dropped out in the horizontal direction is vertically arranged in the adjacent line to perform vertical correlation processing. As a result, the three primary colors, R, G, and B, are processed at the same time.

The missing pixels in the horizontal direction are completely replaced in the vertical direction to obtain improved camera characteristics.

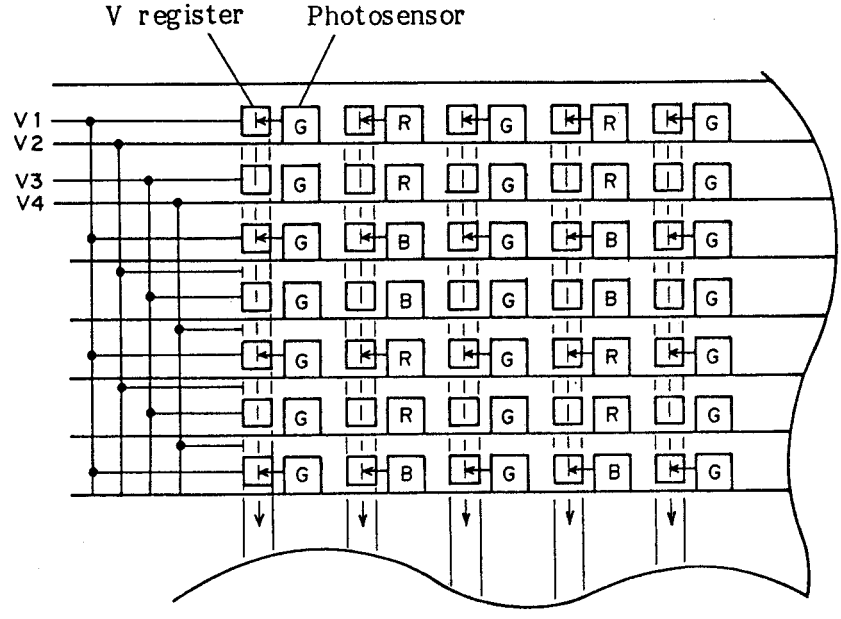
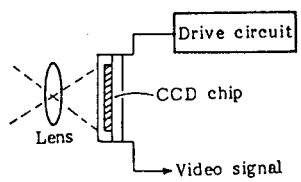


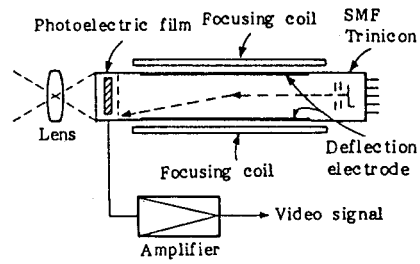
Fig. 1-2 Pixel Arrangement and 4-Phase Driving

Comparison of Solid-State Image Sensor and Pick-Up Tube

	Solid-state image sensor (CCD)	Pick-up tube
1. Life and reliability	Long life possible.	The heater deteriorates with time due to beam radiation.
2. After-image and burning	No after-image. No burning occurs even when the identical object is shot for a long time, or when exposed to an extremely intense light.	Inevitably occurs because or photoelectric film characteristics.
3. Geometrical distortion-free	The regularly arranged pixels and self scanning operation provide an exact geometrical pattern.	Exact beam scanning between pixel and self-scanning the center and peripheral portions is difficult.
4. Vibration and shock resistance	Robust because of the semiconductors used.	Weak because of the glass tube, filament, and socket used.
5. Image display time	Rapidly appears because heater is not required.	Heater warming time is required.
6. Dimensions and weight	Compact and lightweight.	Distance for firing beams is required. Space is also required for deflection and focusing coils.
7. When used in electric and magnetic fields	Not influenced.	Electron beams are influenced.
8. Power consumption	Low-power consumption because of its semi-conductor configuration.	High-power consumption because of the heater, coils, and high voltage used.



CCD camera structure



Pick-up tube camera structure

2. CCD PRINCIPLES

A Charge Coupled Device (CCD) is a semiconductor storage device containing regularly arranged MOS capacitors. It processes electric charges according to the following functions:

2-1. Photoelectric Conversion (An electric charge is generated using light.)

When light strikes the surface, an electric charge proportional to its strength is generated. Fig. 2-1 shows the MOS capacitor structure.

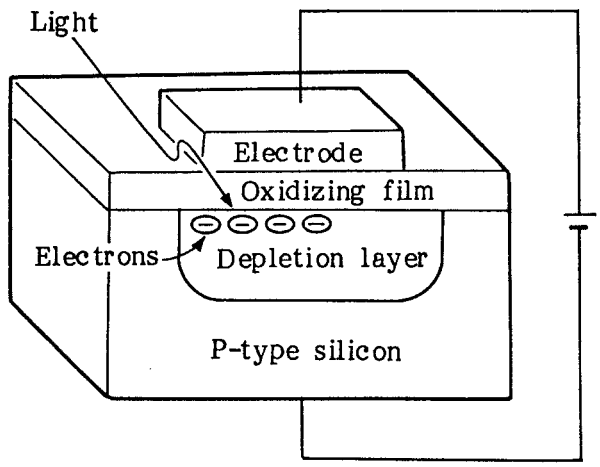


Fig. 2-1 MOS Capacitor

2-2. Charge Storage

When a positive voltage is applied to an electrode of an MOS capacitor, a "potential well" appears on the surface of the P-type silicon located below the electrode. An electric charge can be stored in the potential well.

The electric charge which is generated by photoelectric conversion is stored in the potential well for 1 frame (1/30sec). The resultant charge is then read out of the CCD device using the transfer function described below.

2-3. Charge Transfer (An electric charge is transferred.)

The MOS capacitor row, that is, CCD has a charge transfer function.

The higher the positive voltage applied to the electrode of the MOS capacitor is, the deeper the potential well is.

When different voltages are applied to the electrodes of two adjacent MOS capacitors, potential wells of different depth can appear below the electrodes, and the stored charge moves to the deeper potential well.

The above operation theory is used for the CCD charge transfer.

Fig. 2-3-1 shows the 3-phase CCD operation. Fig. 2-3-1 (a) presents the structure model, and Fig. 2-3-1 (e) the waveforms of the voltage applied to the 3-phase electrodes P1, P2, and P3.

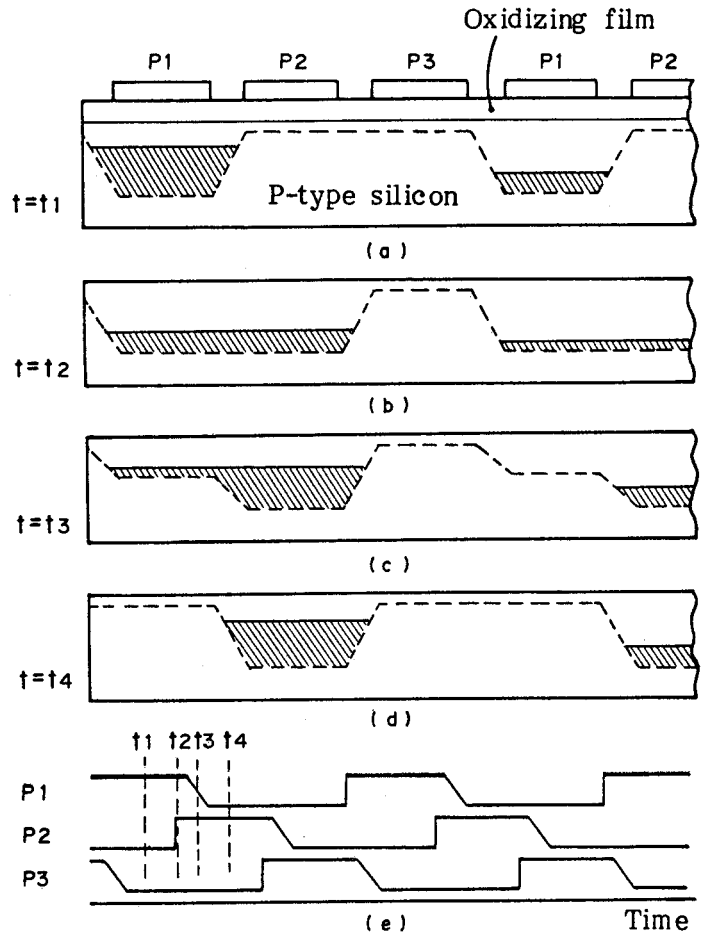


Fig. 2-3-1 Electric Charge Transfer

2-4. Device Structure

The silicon substrate employs a P-type high-resistance substrate based on the recently developed Magnetic Field Applied Czochralski (MCZ) method.

A P-type barrier is formed under the N-type embedded channel CCD to considerably reduce smear which passes through the silicon substrate from the photosensing pixel portion, leaks to a vertical transfer CCD, and appears as a vertical stripe on the screen.

The short-wavelengh sensitivity of the photosensing pixel portion is improved by a multiple interference effect of the silicon substrate with an SiO2 film, multi-crystalline silicon film, and Si-N film.

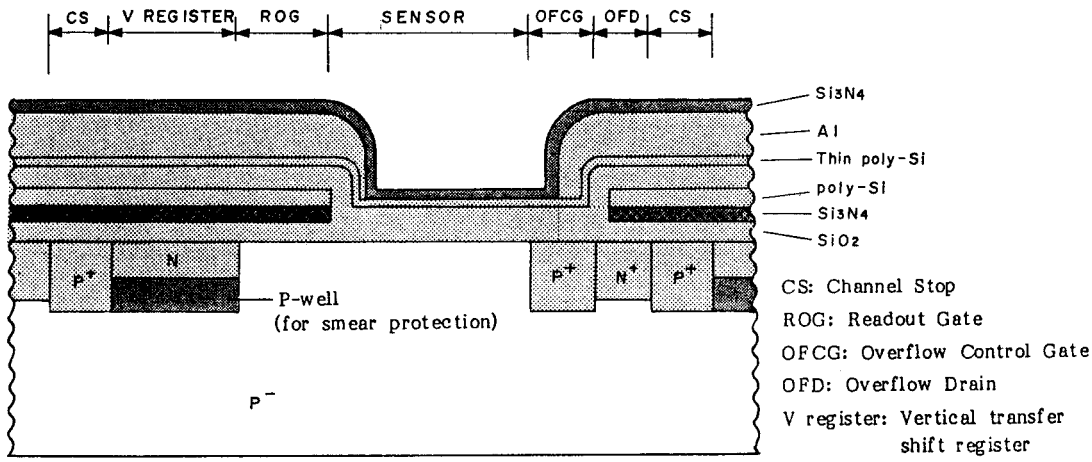


Fig. 2-4-1 Horizontal Sectional View of ICX018 (021)

2-5. Interline Transfer Mechanism

The alternating photosensitive pattern and vertical transfer register are connected using a horizontal transfer register.

Light is sent to the photosensitive portion, and an electric charge proportional to its brightness is generated.

The resultant charge is moved to the vertical transfer register all at once, then sequentially moved to the horizontal transfer register. Finally, the electric charge is sent to an output amplifier and read as a signal.

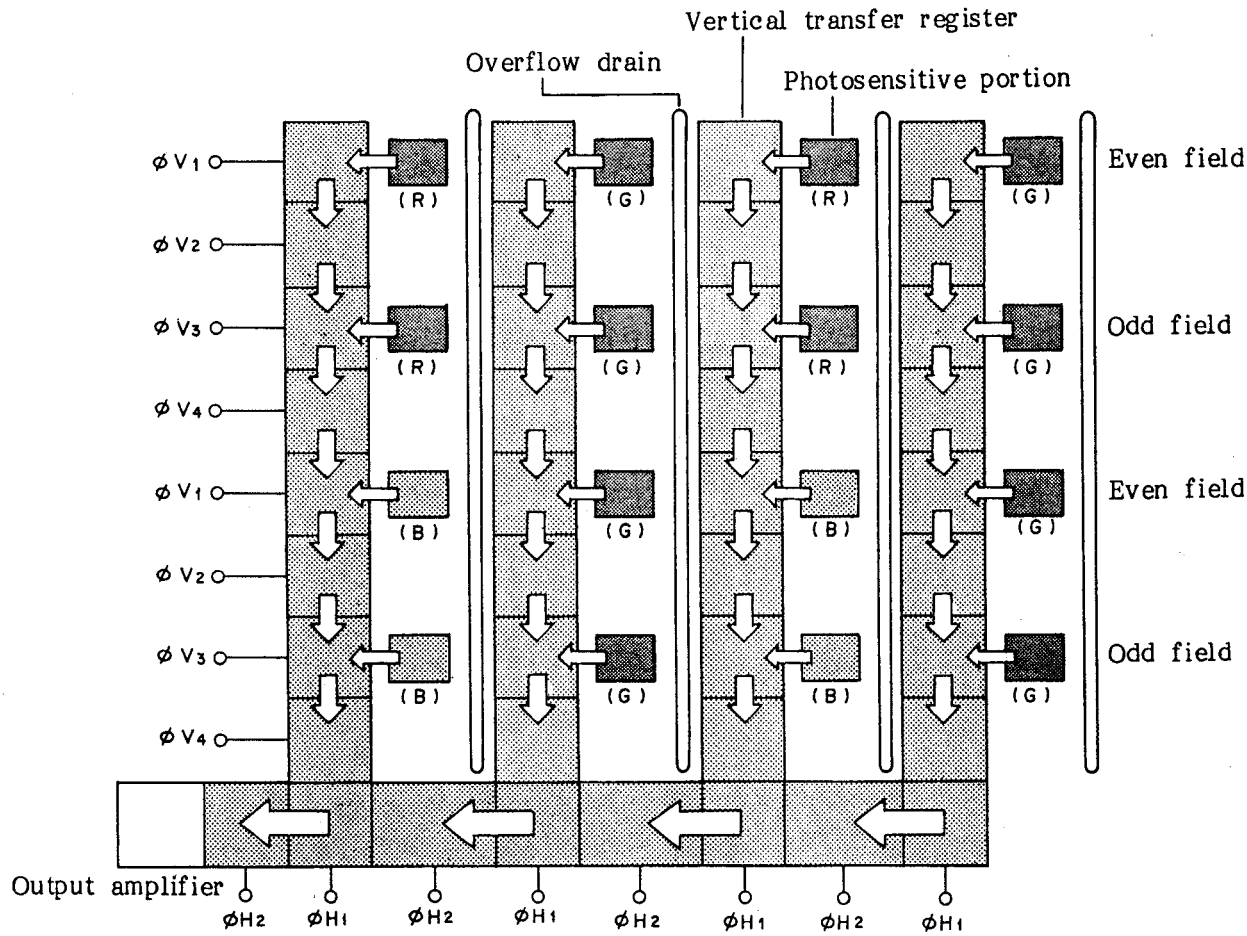


Fig. 2-5-1 Horizontal Transfer Register (CCD)

As shown in Fig. 2-5-2, the photosensor and transfer register are separated in the interline transfer system. The signal charge is sequentially transferred to the photosensor, vertical register, and horizontal register, then output from the output portion.

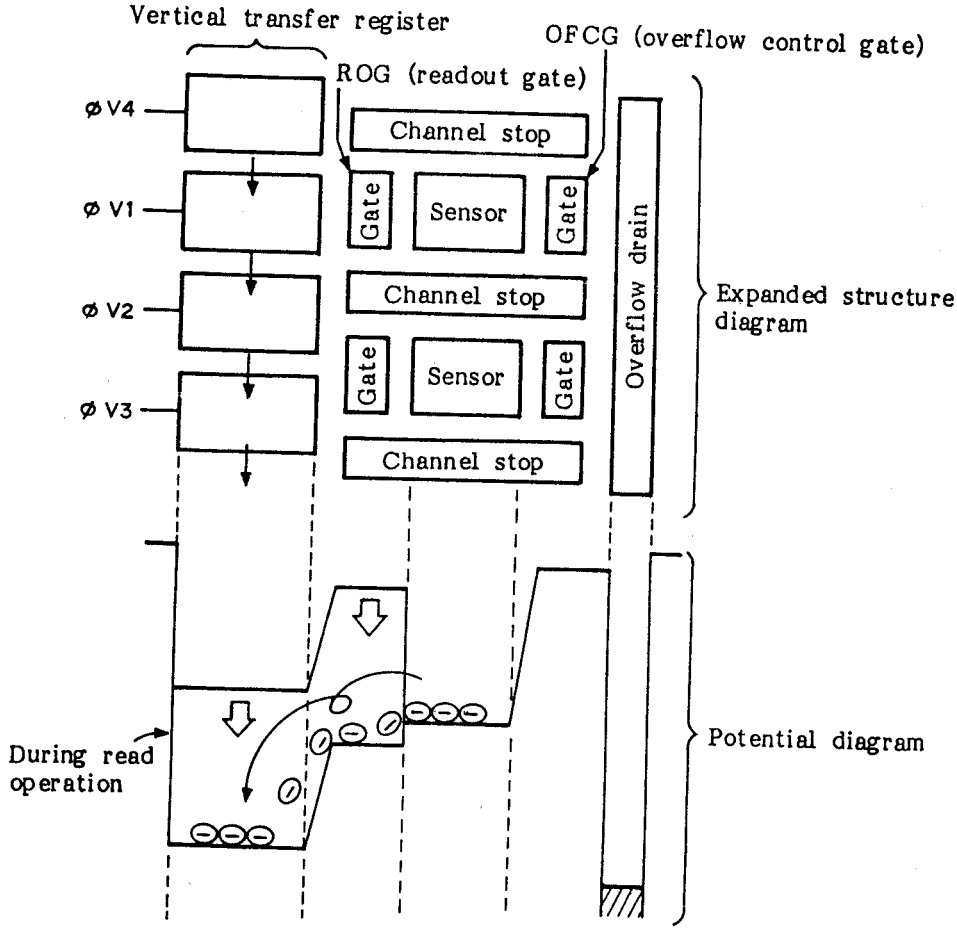


Fig. 2-5-2 Expanded Cell Structure Diagram and Potential Diagram

2-6. Tristate Driving Signal Read Operation from Sensor

This unit employs a vertical register tristate driving system which eliminates the need for the miniaturized sensor to partially send a signal to portions other than a vertical register during read operation.

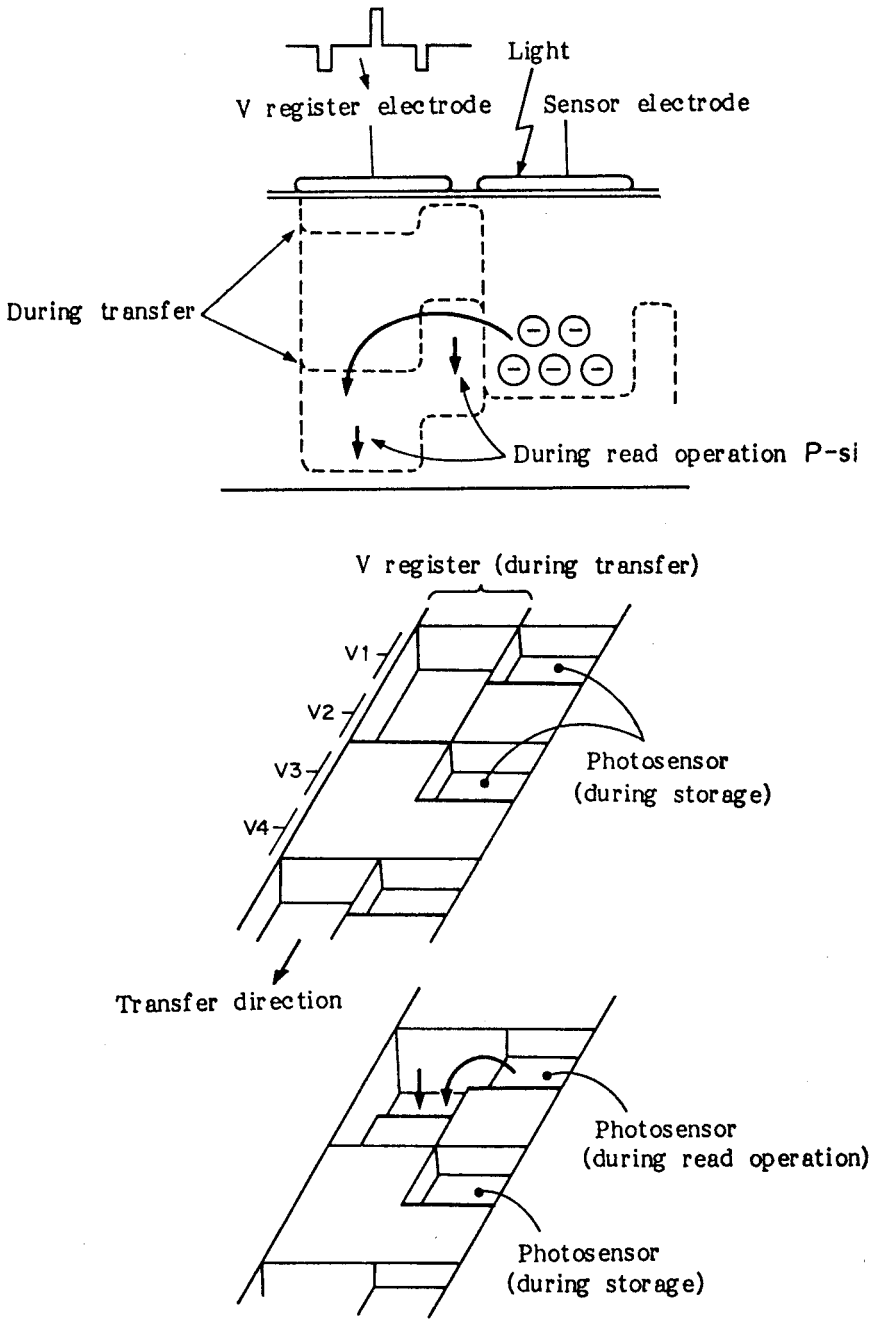


Fig. 2-6-1 Tristate Driving Read Operation

2-7. Sensor to Vertical Register Transfer Mechanism

The transfer of a signal from a sensor to a vertical register is described here with reference to Fig. 2-7-1.

The potential of the sensor is increased by the 10V dc which is applied to the SG pulse at all times.

The potential is in the photosensing storage state at timing A1. V1 is +12V at timing B1. Therefore, the potential of the vertical register is increased.

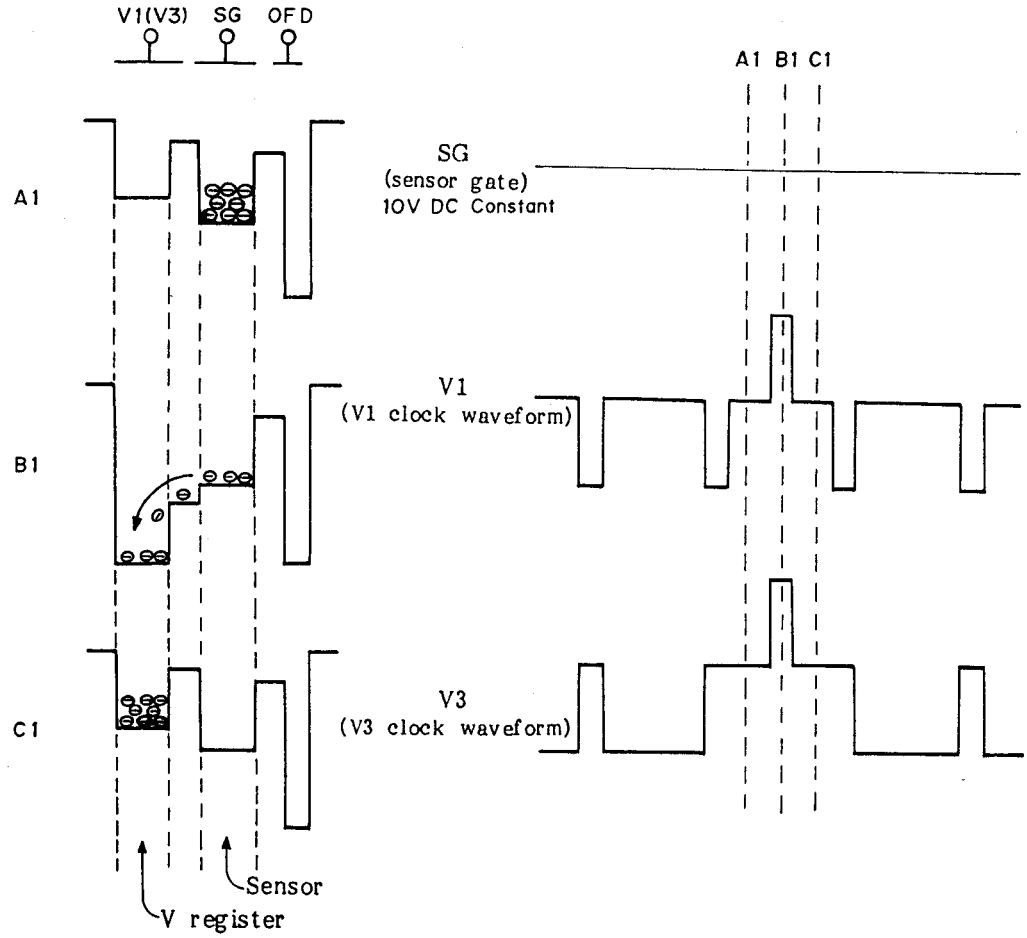


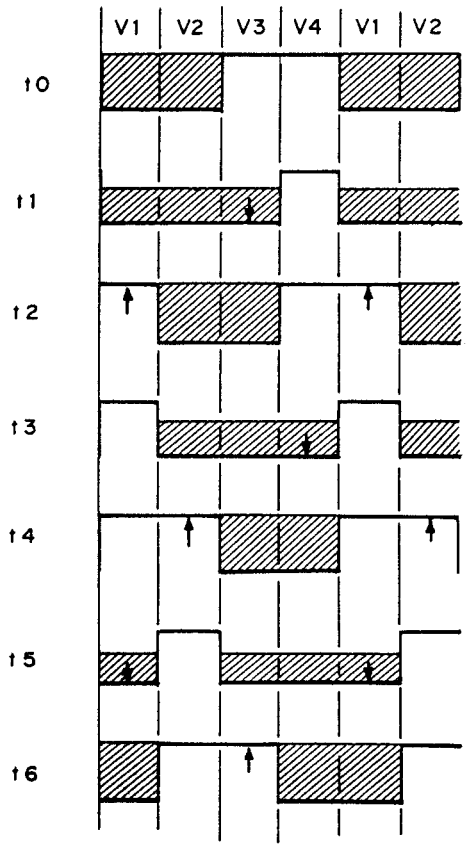
Fig. 2-7-1 Sensor to Vertical Register Transfer Mechanism

At B1, the electric charge is moved from the photosensor to the vertical register. V1 is decreased again at timing C1, so the potential returns to the photosensing storage state.

2-8. Tristate 4-Phase Driving Operation (Vertical Driver)

This system containing the large number of pixels requires the mechanical width of the vertical register to be reduced. The maximum electric charge is decreased in a 2-phase driving system. Therefore, this unit employs a 4-phase driving system.

. 4-phase driving system model



	4-phase
Merits	. Many charges can be handled at an electrode. . The cell can be miniaturized for the same dynamic range as in a 2-phase driving system.

Fig. 2-8-1

2-9. Vertical Register to Horizontal Register Charge Transfer

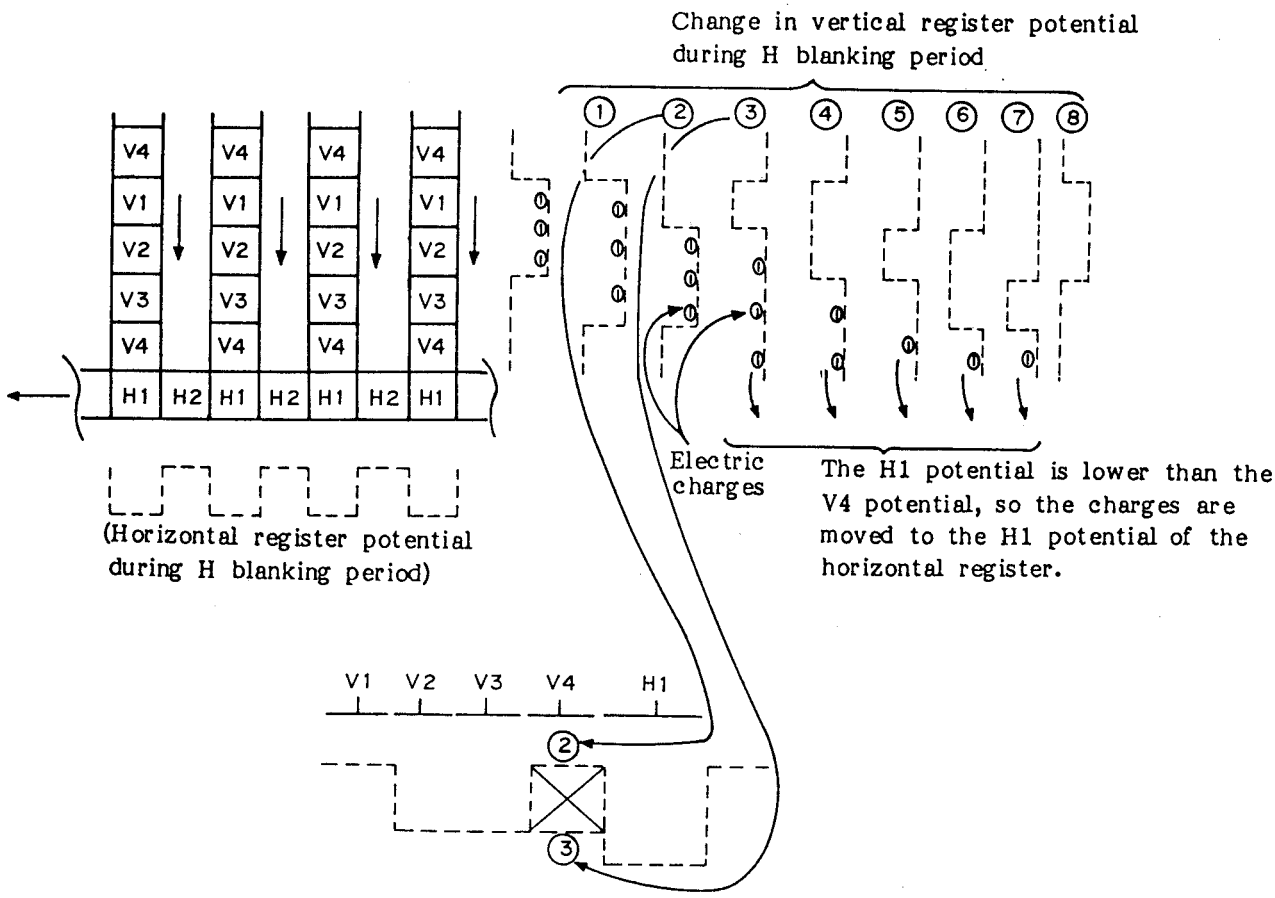


Fig. 2-9-1 Potential Diagram of Horizontal and Vertical Registers

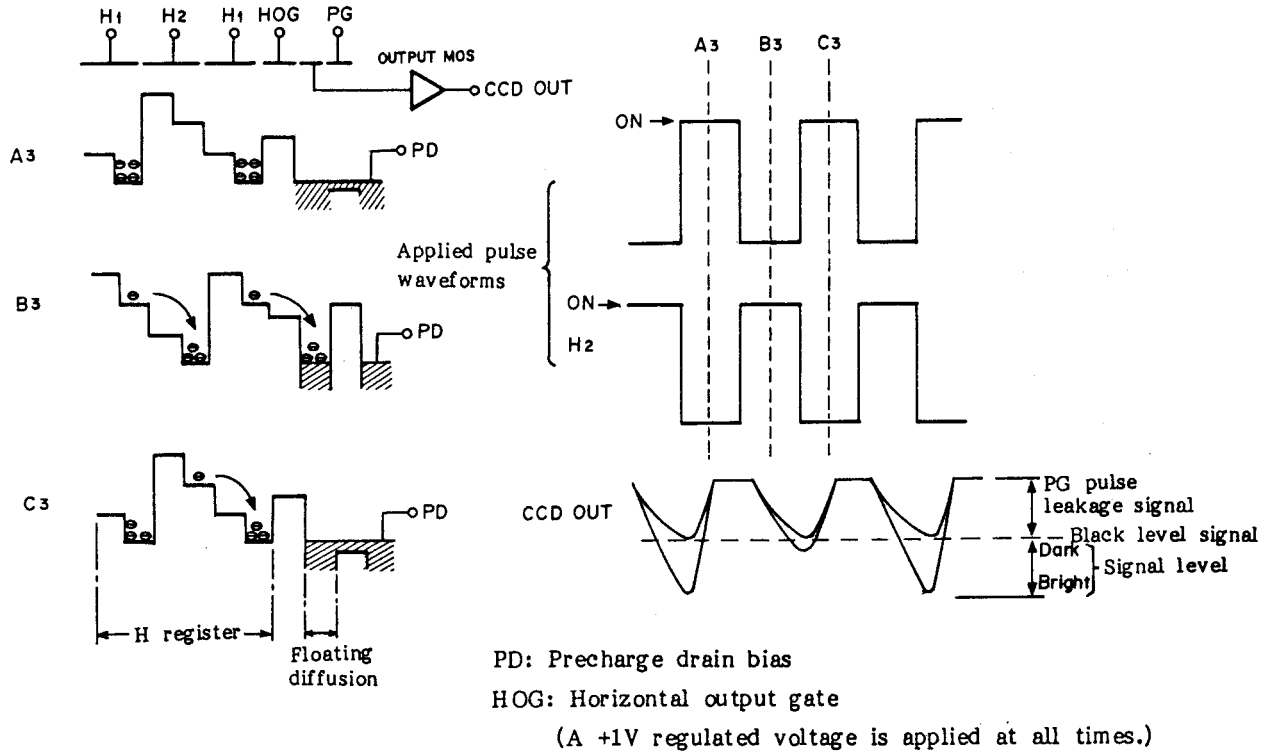
As shown in Fig. 2-9-1, the H1 potential of the horizontal register goes low (the potential well is deepened) during the H blanking period. At that time, the horizontal register becomes ready to receive a signal from the vertical register.

The vertical register which is stopped at low V1 and V2 potentials during the H display period performs a one-line transfer during the H blanking period, following the 4-phase driving operation shown in (1) through (8) of the above illustration. V4 functions as a Vertical Output Gate (VOG) during the transfer operation and controls the transfer of a charge from the vertical register to the horizontal register.

2-10. Horizontal Register to Output Portion Transfer Mechanism

The electric charge sent to the final stage of the horizontal register is transferred to floating diffusion (refer to the figure below).

H1 and PG pulses are turned on at timing A3, and the floating diffusion is reset to the PD pulse charge. H1 and PG pulses are turned off at timing B3, and the charge is moved to the floating diffusion with the shallower potential.



PD: Precharge drain bias

HOG: Horizontal output gate

(A +1V regulated voltage is applied at all times.)

Fig. 2-10-1 Horizontal Register to Output Portion Transfer Mechanism

The electric charge is converted into a voltage at a ratio of V = Q/C in accordance with equivalent capacity C of the floating diffusion. H1 and PG pulses are turned on again at timing C3, and the floating diffusion is reset to the PD potential.

2-11. Signal Extraction Principles

The CCD output stage is represented by the equivalent circuit in Fig. 2-11-1, where

- SW is switched using a PG pulse,
- C is equal to floating diffusion and
- The source follower is equal to an output MOS.

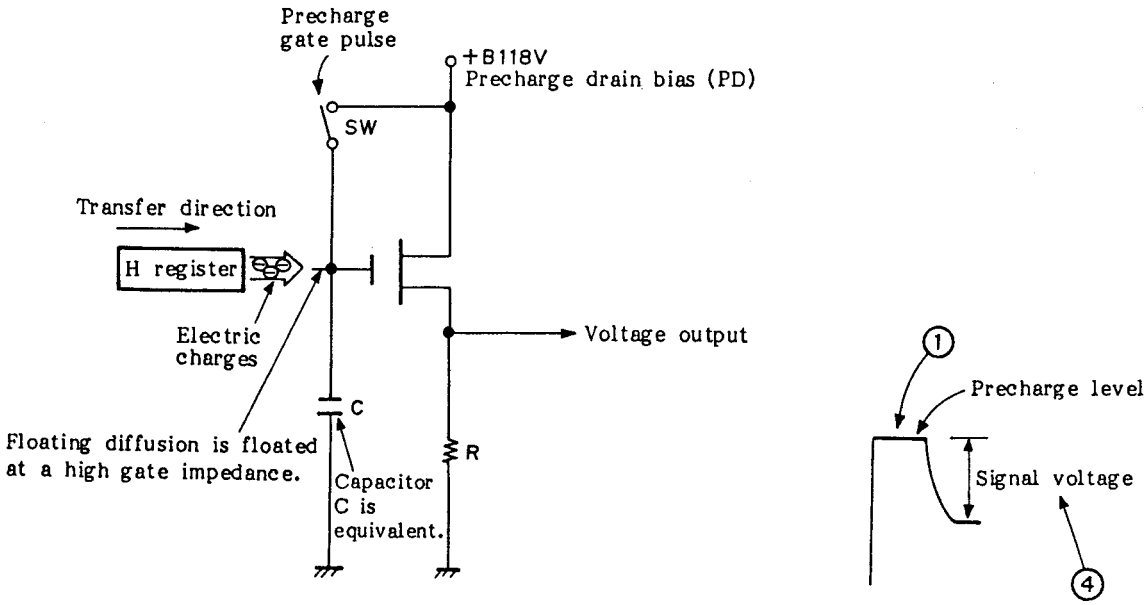


Fig. 2-11-1 Signal Extraction Principles

The circuit operation is described here based on the signal extraction principles.

(1) Switch SW is turned on and capacitor C is charged using a +B voltage (PD voltage).

(2) Switch SW is turned off. The floating diffusion is then floated at a high impedance.

(3) The electric charge is transferred using a horizontal register.

(4) The electric charge on capacitor C is discharged and the voltage level at the gate is decreased. Therefore, the voltage level at a source is decreased. When intense light is sent to the imager, the stored charge and the signal voltage level are also increased.

2-12. Vertical Correlation Processing

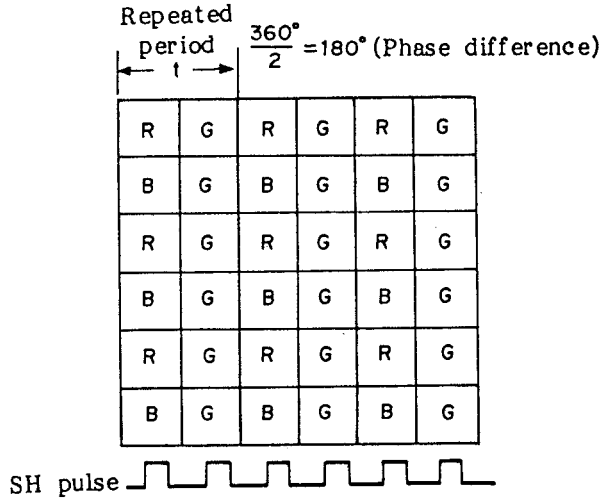


Fig. 2-12-1

The color filter-arranged CCD imager shown in Fig. 2-12-1 produces only two chroma signals R and G (or B and G). To create a color TV signal, three chroma signals, R, G, and B, are required at the same time. The missing chroma signals can be compensated using a 1H- or 2H-signal during the vertical period. This compensation method is called vertical correlation processing, as shown in Fig. 2-12-2.

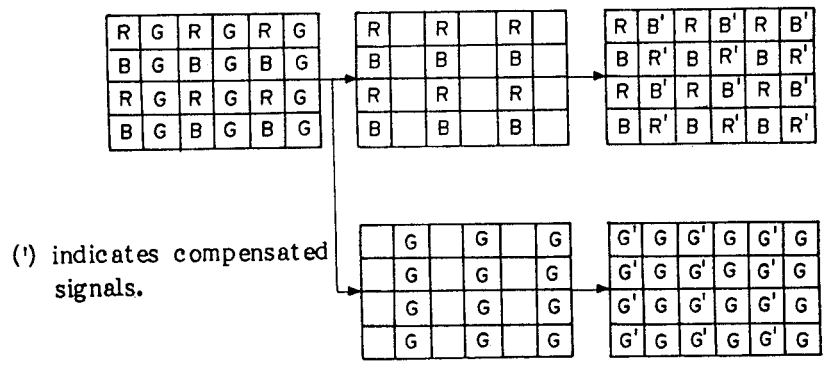


Fig. 2-12-2

Vertical correlation processing requires a 1H-delay line, so this system has a 1H-delay line consisting of CCD (CX23039).

The false signal which is generated due to the limited number of pixels is processed and compensated to produce a chroma signal component. The low-frquency range (YL) of the Y (luminance) signal constitutes a matrix in accordance with YL = 0.36R + 0.59G + 0.11B. As shown in Fig. 2-12-3, the resultant Y signal consists of low-frequency and high-frequency ranges.

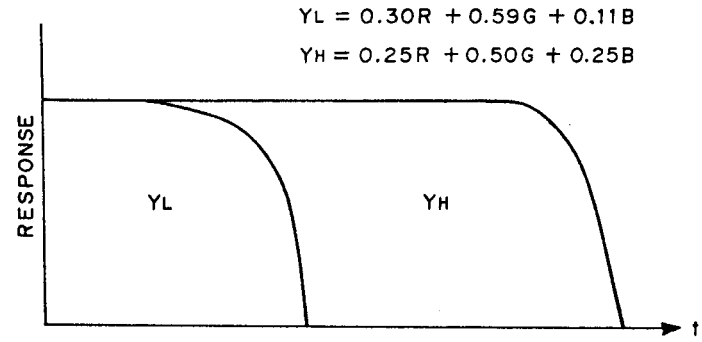


Fig. 2-12-3

The high-frequency range (YH) of the Y signal has an equivalently improved resolution in accordance with YH = 0.25R + 0.50G + 0.25B. The YL and chroma signal component (R-Y, B-Y) have high color reproducibility.

2-13. Sampling

In this system, the solid-state image sensor employing CCDs has a photosensing surface consisting of a two hundred and fifty thousand element-array optical data is modulated through the array. This is called an optical sampling. As shown in Fig. 2-13-1, the input optical data is partially extracted in accordance with the number of pixels.

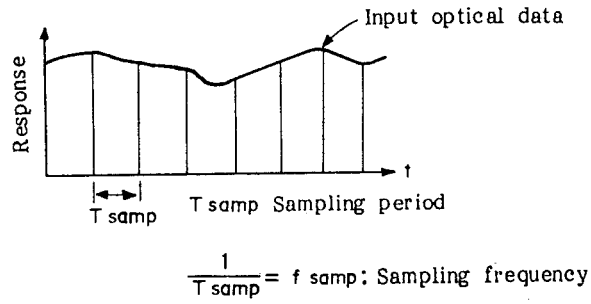


Fig. 2-13-1

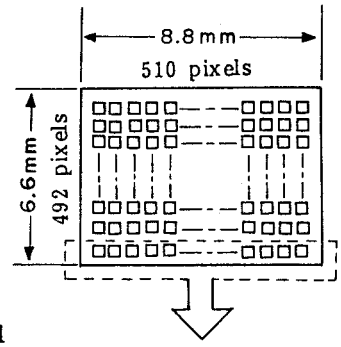
The extraction period is called a sampling period (T samp).
The resolution of a CCD solid-state image sensor is determined by the sampling frequency f samp (1/T samp), and the resolution at the video camera block is determined by the number of pixels. For ICX018 (NTSC), sampling frequency fs is as described below.

$$fs = \frac{\text{Effective number of pixels}}{\text{Effective scanning time}} = \frac{510}{53.63(\mu s)} \fallingdotseq 9.51(MHz)$$

Actually, sampling frequency fs is 9.55MHz because 28.63636MHz is frequency-divided by three. The 9.55MHz frequency is used as a signal sampling frequency. This system employs a two pixel-pitch color filter, so the sampling period for color separation is

$$\frac{9.55}{2} \fallingdotseq 4.77(MHz)$$

(a) CCD solid-state image sensor



(b) Pixel array on one horizontal scanning line

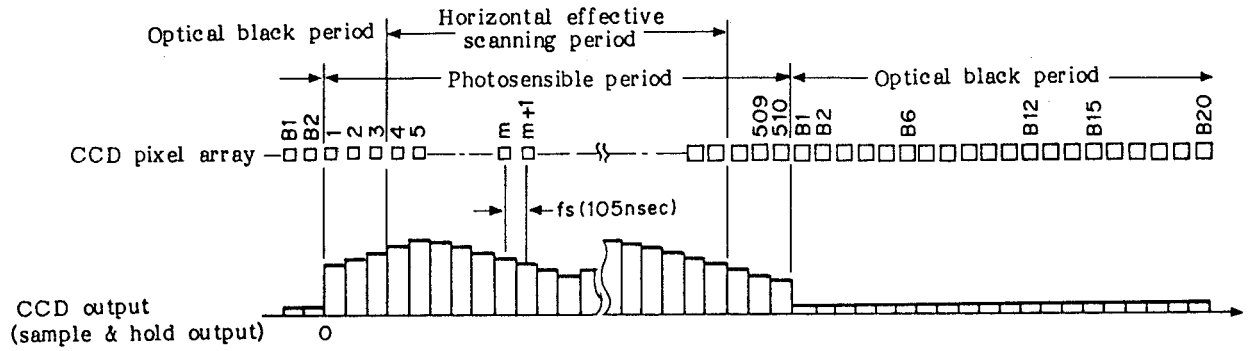


Fig. 2-13-2 Solid-State Image Sensor and Pixel Array on Horizontal Scanning Line

Optical data which is sent to the CCD image sensor surface is sampled using the pixels arrayed in the horizontal and vertical directions. The small number of pixels drops a part of data, so more pixels are required. The CCDs read the spatially sampled data as a time function in accordance with the self-scanning operation.

2-14. Reflected Distortion

(1) The reflected distortion is a false signal fA = fs - f which is generated when an original signal of frequency f is sampled using frequency fs < 2f.

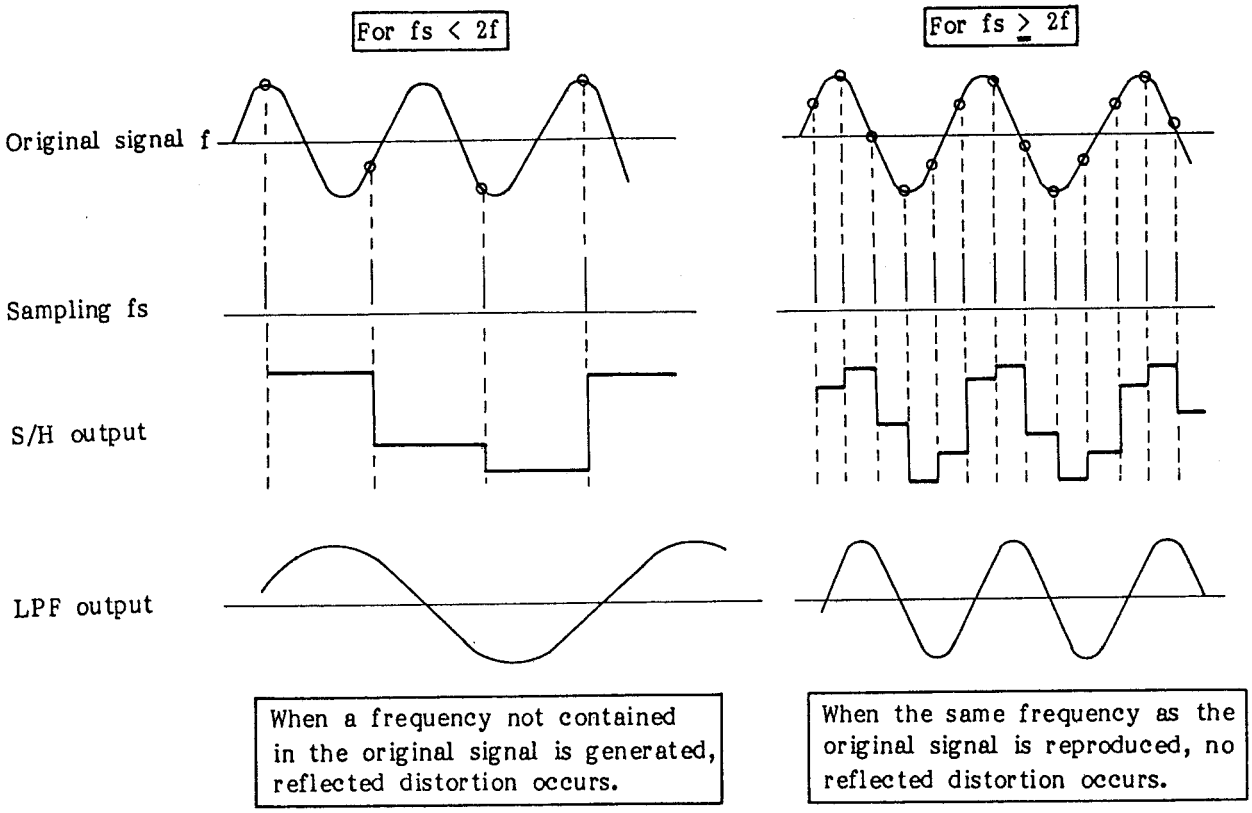


Fig. 2-14-1

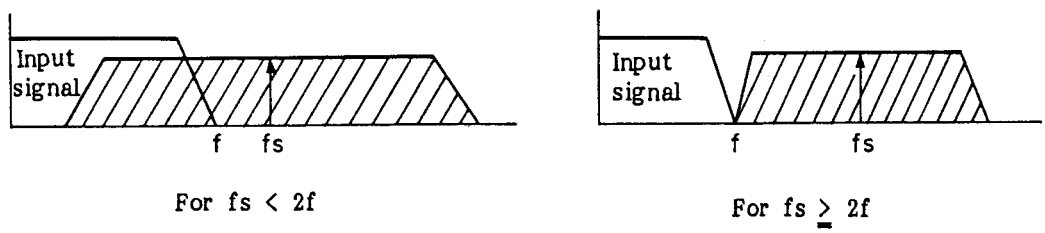


Fig. 2-14-2

As shown in Figs. 2-14-1 and 2-14-2, when fs ≥ 2f, no reflected distortion occurs.

(2) When the input is sampled at more than two times its maximum frequency f, no reflected distortion occurs in the original frequency range (sampling theorem). In this case, fs is the sampling frequency.
To prevent the reflected distortion caused by sampling, the maximum frequency of an optical image must be limited to fs/2 in accordance with the sampling theorem. Therefore, an optical low-pass crystal filter is provided. The signal frequency range is shown in Fig. 2-14-3.

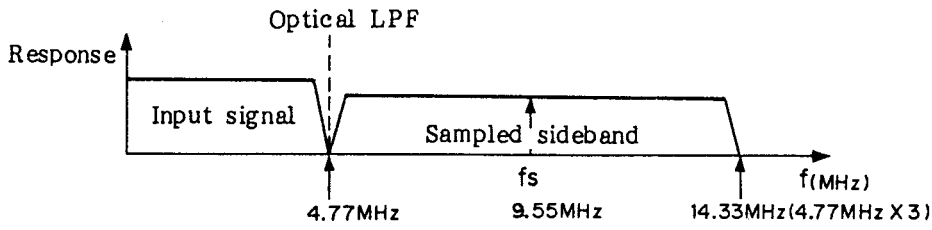


Fig. 2-14-3

3. CCD BLOCK ON BI-3 BOARD

The NTSC system employs ICX018, and the PAL system ICX021.

The block diagram and terminal pins are described here. For further imformation on pulse waveforms, refer to PG-12 in Section 10.

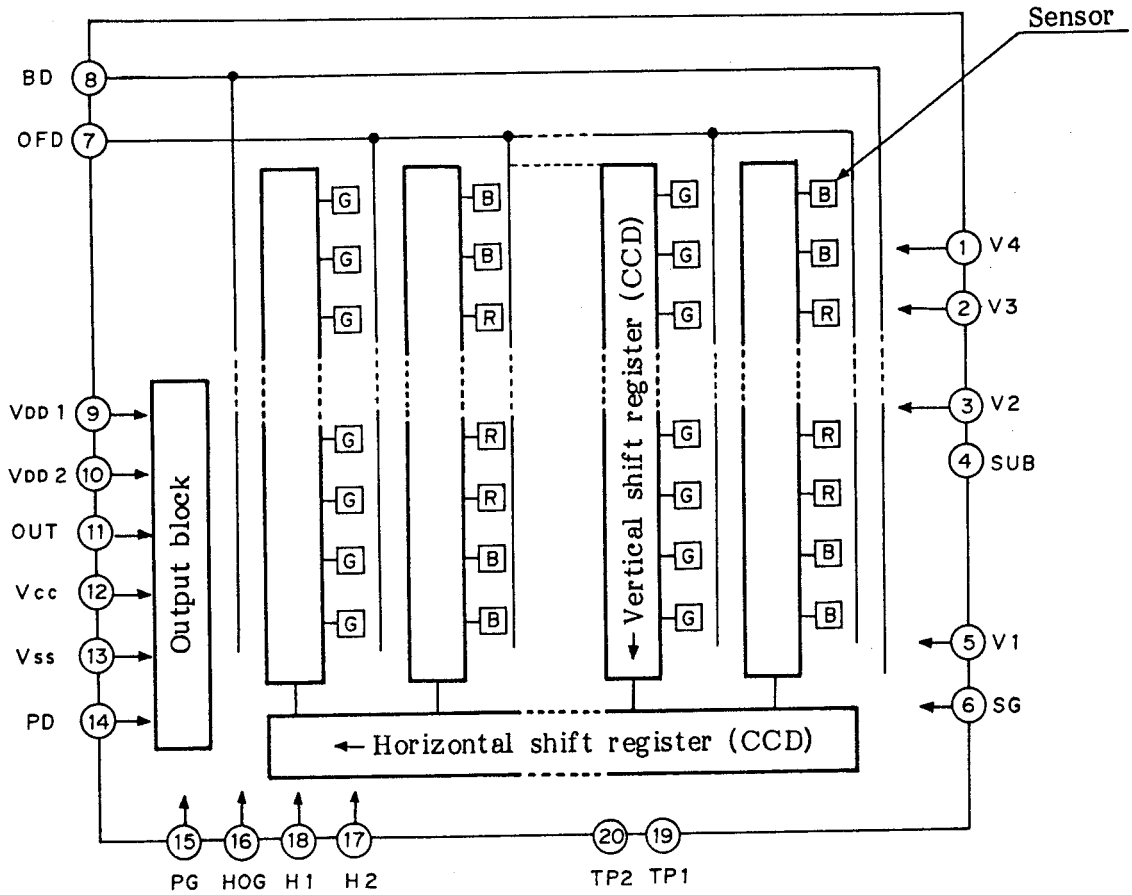


Fig. 3-1

Pin No.	Symbol	Description
1	Vø4	Vertical register transfer clock input
2	Vø3	Vertical register transfer clock input
3	Vø2	Vertical register transfer clock input
4	SUB	GND
5	Vø1	Vertical register transfer clock input
6	SG	Sensor gate bias
7	OFD	Overflow drain
8	ED	Edge drain bias
9	VDD1	Supply voltage
10	VDD2	Supply voltage
11	OUT	Signal output
12	VCC	Output amplifier gate bias
13	VSS	Output amplifier source bias
14	PD	Precharge drain bias
15	PG	Output reset clock input
16	HOG	Horizontal register read control bias
17	H2	Horizontal register transfer clock input
18	H1	Horizontal register transfer clock input
19	TP1	Test pin
20	TP2	Test pin

4. SIGNAL SEPARATOR CIRCUIT ON MB-37 BOARD

4-1. Outline

The output from the BI-3 board is directly input to the signal separator circuit on the MB-37 board. A precharge pulse is then eliminated, and only a signal is extracted.

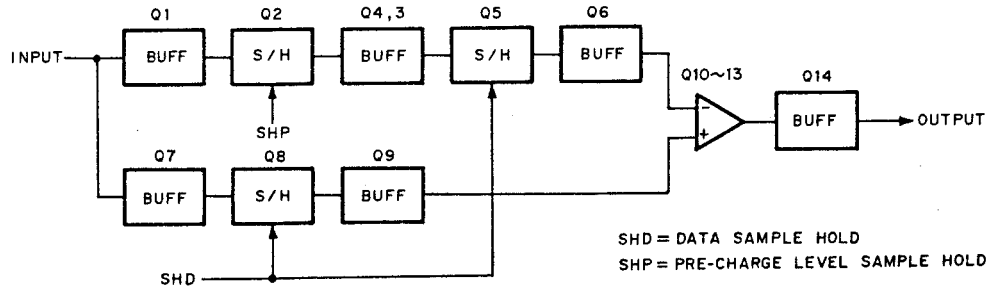


Fig. 4-1-1

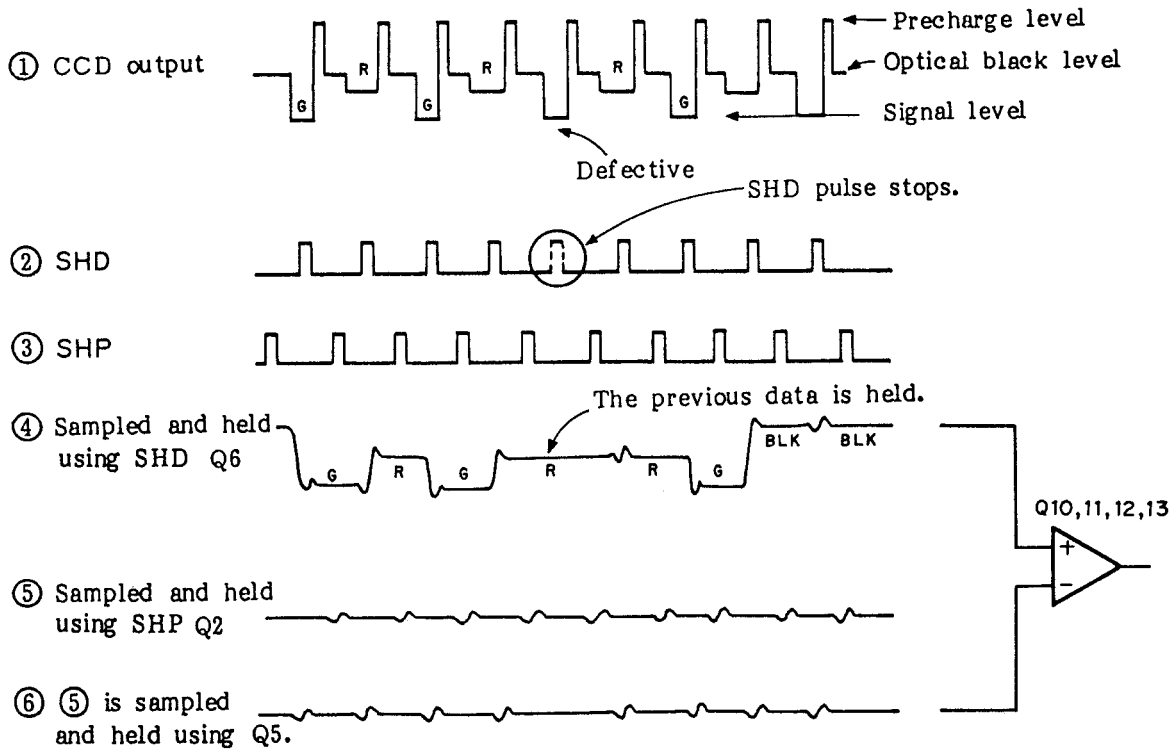


Fig. 4-1-2

4-2. Signal Sample & Hold

The output from CCD is passed through buffer Q7, and the signal level is sampled and held through DHD using Q6 ((4)). The resultant signal is then passed through buffer Q9 and input to the plus side of a differential amplifier consisting of Q10 and Q11. If defects are found in the CCD, SHD is stopped and the previous signal level is output. The defective CCD location is written into the ROM, and the timing pulse generator is controlled so that the defective CCD can be compensated as required.

4-3. Precharge Level Sample & Hold

The output from CCD is passed through buffer Q2, and the signal level is sampled and held through SHP using Q2. The resultant signal output is shown in (5) of Fig. 4-1-2. The sample and hold operation is perfomed using a transistor, so spike noise appears at the switching point during signal output. Output (5) is then passed through a buffer consisting of Q3 and Q4, and its waveform is sampled and held through SHP using Q5. Conseqently, the signal sample and hold operation can be perfomed at the same timing.

Output (5) is sampled and held in output (6) using Q5. The resultant output signal is passed through buffer Q6 and input to the minus side of a differential amplifier consisting of Q10, Q11, Q12, and Q13.

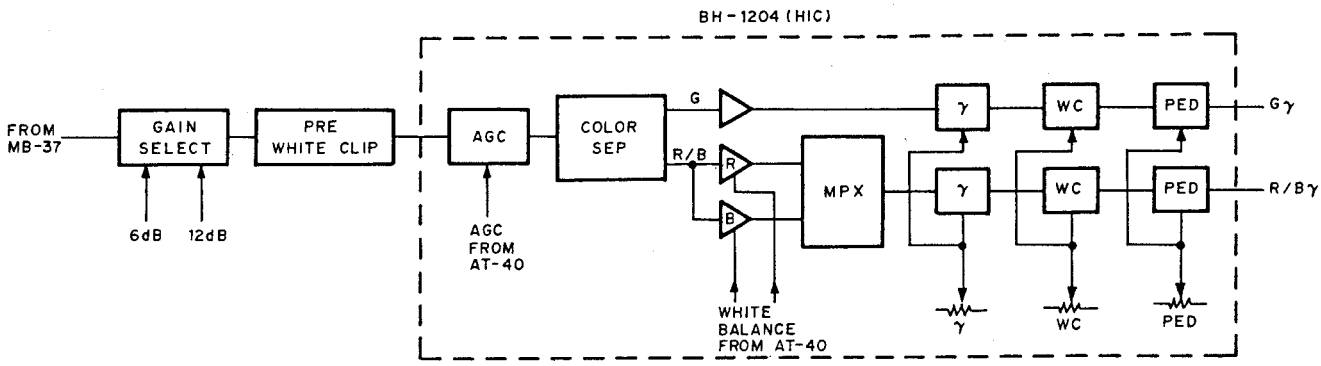
4-4. Differential Amplifier

The differential amplifier consisting of Q10 through Q14 is used to extract the signal component and eliminate the in-phase noise component.

Since the signal sample and precharge level sample have the same phase and timing, the spike noise generated by the sample and hold transistor can be canceled by the differential amplifier.

5. PROCESS CIRCUIT ON PR-72 BOARD

5-1. Outline



The PR-72 board configuration is shown in the above block diagram.

Fig. 5-1-1

5-2. Gain Selection and Gain Selection Command

5-2-1. Gain selection

The output from the MB-37 board is sent from pin 5 on the PR-72 board and input to a gain control circuit (with gains of 0dB, 6dB, and 12dB) consisting of Q4 and Q5.

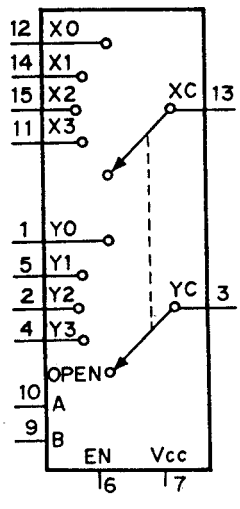
When the control circuit is set to 0dB, Q4 and Q5 are turned off and the signal is sent through C5 and R26 to the emitter of Q5. When set to 6dB, Q4 is turned on, and C6, C7, and R27 are connected in parallel with C5 and R26 with the gain raised by 6dB. When set to 12dB, Q5 is turn on, and C18, C19, and R28 are connected in parallel with C5 and R26.

The outut from the gain control circuit is passed through amplifier Q6 (with approximately unity gain), buffer Q7, clamp circuit Q8, and buffer Q9, then clipped using a pre-white clipping circuit and fed to BH1204 (IC4).

5-2-2. Gain selection command

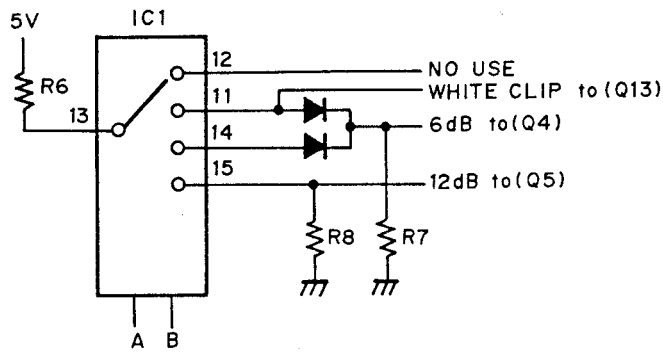
A two-bit gain control signal is input from pins 30 and 31 on the PR-72 board. The resultant signal is input to the control terminal of demultiplexer IC1 to control a transistor in accordance with each gain mode.

IC1 TC4052BF



0 : LOW LEVEL
1 : HIGH LEVEL
X : DON'T CARE.

CONTROL INPUTS			"ON" CHANNEL
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	X	X	OPEN



Gain selection

Gain		A	B		Selection
0dB		0	0		Pin 12
6dB		1	0		Pin 14
12dB		0	1		Pin 15
AUTO		1	1		Pin 11

Fig. 5-2-1

5-3. IC4 (BH1204)

IC4 CX20035 performs various signal processes.

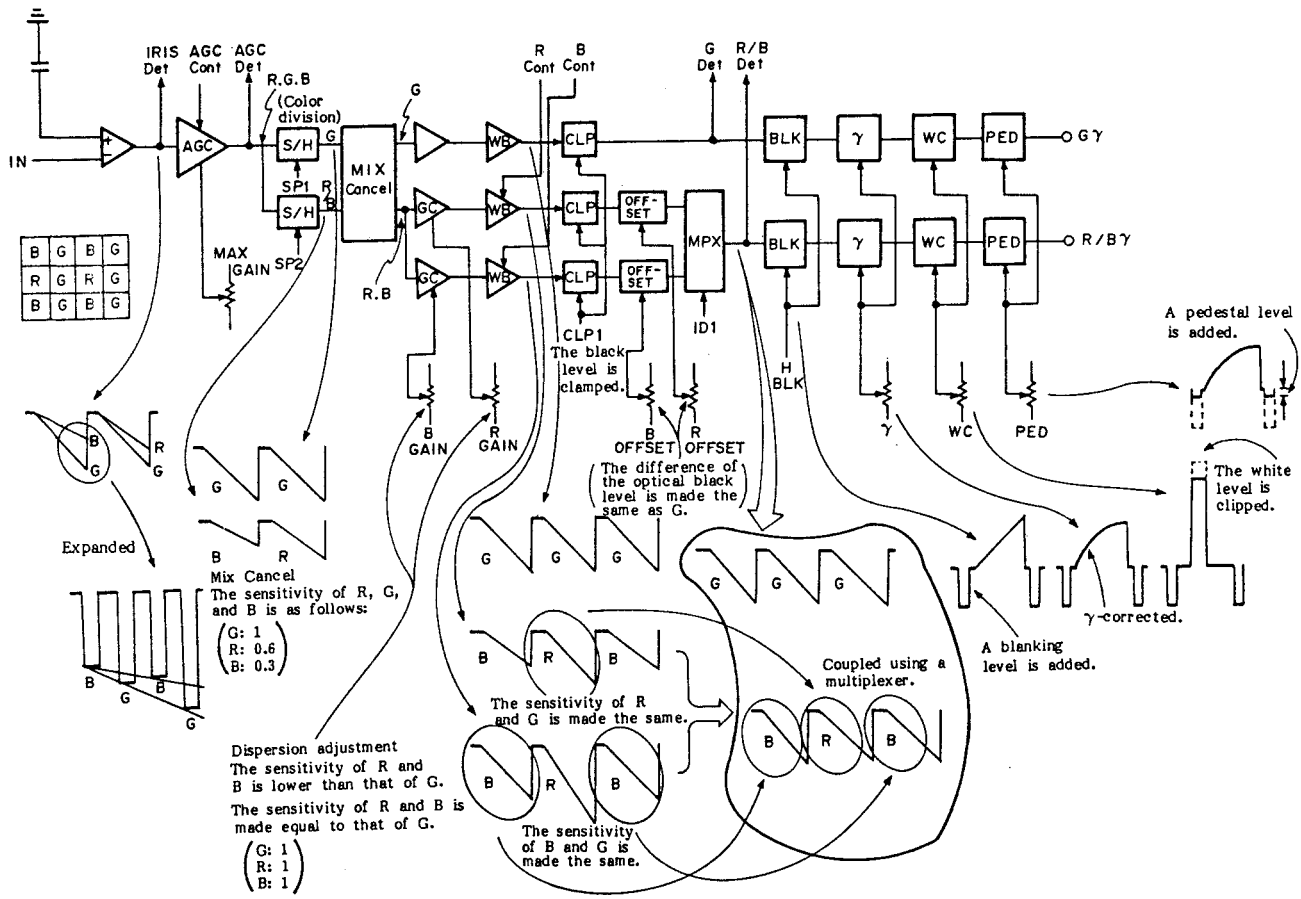
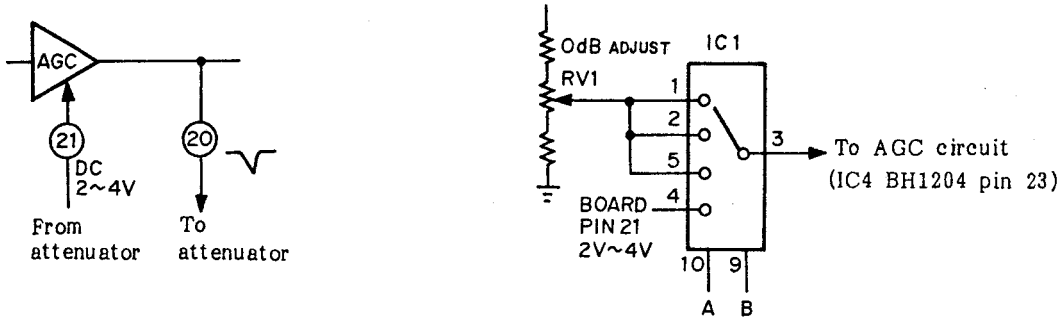


Fig. 5-3-1 CX20035 Block Diagram

5-4. Automatic Gain Control (AGC)

The AGC amplifier is provided in IC4 (CX20053) to amplify the output level to 0dB when the amount of incident light is low.

The output of the AGC amplifier is sent from pin 20 to the AT-40 board. The AGC amplifier control signal corresponding to the detected signal level is input from pin 21 at 2 to 4V dc and sent to IC1.



AGC selection

Mode		A	B	Selection
AUTO		1	1	Pin 4
6dB		1	0	Pin 1
12dB		0	1	Pin 2
0dB		0	0	Pin 5

Fig. 5-4-1

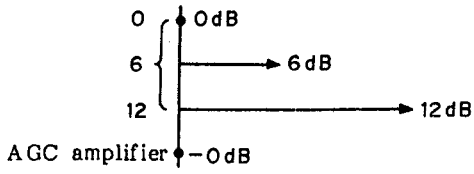
When 0dB, 6dB, and 12dB are selected using the gain mode select switch, IC1 produces the voltage determined by RV1. The resultant signal voltage is fed to the AGC amplifier (CX20053). In this case, the AGC amplifier (CX20053) gain is 0dB.

When AUTO is selected (at pin 4 of IC1), the voltage at pin 21 is input to the AGC amplifier (CX20053). At that time, the AGC amplifier gain is changed in the range of -6 to +3dB in accordance with the DC voltage. Moreover, when 0dB, 6dB, and 12dB are selected, Q4 is turned on for +6dB-amplification to adjust the gain.

Since the gain is amplified by +6dB using Q4, Q12 and Q13 are used to raise the white clip level of Q12 in the AUTO mode.

AGC amplifier (CX20053) gain

Gain in the 0dB, 6dB, and 12dB modes



Center gain in the AUTO mode

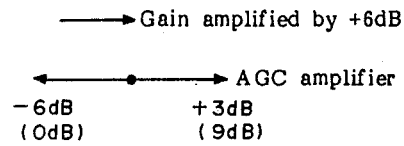


Fig. 5-4-2

When Q13 is turned on and Q12 is turned off, the DC level at the base of Q12 is decreased and the white clip level is increased.

The maximum gain adjustment using RV2 on the PR-72 board is limited so that the total gain in the AUTO mode does not exceed 9dB.

5-5. Color Separator S/H Circuit

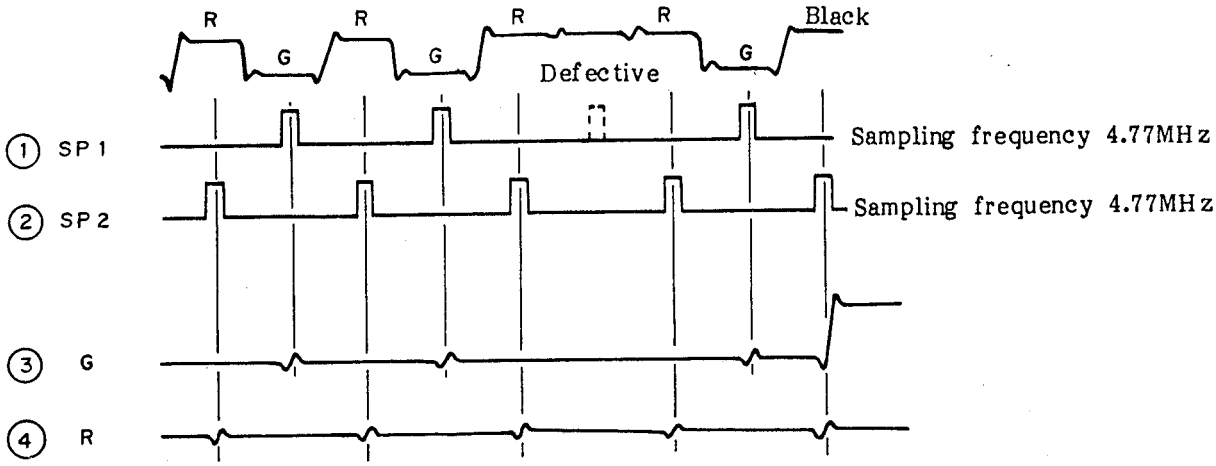


Fig. 5-5-1

The output of the differential amplifier is fed through the AGC amplifier to the color separator S/H circuit. This circuit operates like a signal separator S/H circuit, except that the sampling pulse is replaced from SHD to SP1 and SP2, and the G signal is separated using SP1, and R and B signals using SP2.

When defects are found in the CCD solid-state image sensor, SP1 and SP2 stops the operation by one bit and holds the previous data to compensate for the defective location using the ROM readout and timing generator in IC2 on the PG-12 board.

5-6. Mix Cancel Circuit

The mix cancel circuit consists of Q1, Q2, Q3, and Q11 on the PR-72 board.

When a signal separator circuit is used, R and B signals may leak into the G signal. The mix cancel circuit is used to compensate for crosstalk. For circuit operation, the G signal from pin 20 of IC4 is input to Q1. The R and B signals are also attenuated using R39 and RV6 and sent to Q2 for inversion. In this way, the R and B signals are subtracted from the G signal to cancel the crosstalk. The R and B signal attenuation is adjusted using RV6.

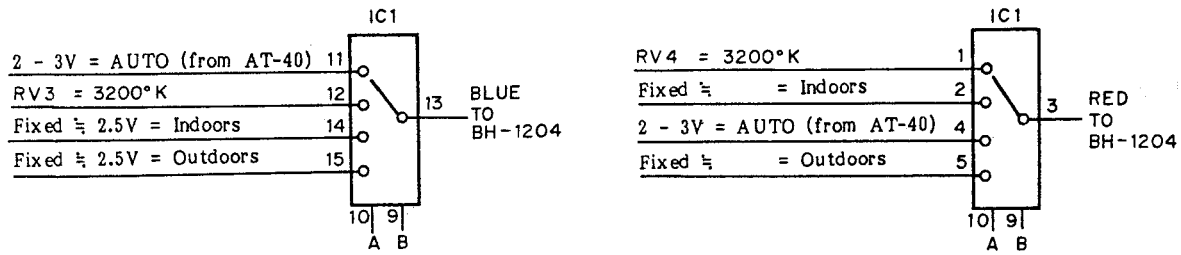
5-7. RB Gain Adjustment

The ratio of the R signal to G signal and the B signal to G signal which are output from the CCD solid-state image sensor varies with the CCD. Therefore, the RB gain is adjusted using RV7 (B) and RV6 (R) in IC4 to absorb the dispersion.

5-8. White Balance Adjustment

The white balance can be selected as follows in accordance with the light source.

(1) 3200° K Tungsten halogen lamp for studio use
(2) Indoors Fluorescent lamp
(3) Outdoors Fine
(4) AUTO white White balance adjustment in the AUTO mode



Color temperature	A	B	Pin No.	
3200° K	0	0	12	1
Indoors	1	0	2	14
Outdoors	0	1	5	15
AUTO	1	1	11	4

Fig. 5-8-1

The DC signal selected using IC1 (TC4052 BF) is passed through buffer IC3 and input to IC4 CX20053 to control the B and R gains in accordance with the selection operation. For AUTO white balance adjustment, the DC signal is input from a B signal at pin 22 and R signal at pin 23 to IC4 through IC2 and IC3. At that time, the input voltage is 2 to 3V dc with the gain changed by ±6dB. Moreover, the DC signal can be input from the external unit to the PR-72 board so as to control the B and R gains.

An input (2 to 3V dc) at pins 28 and 29 is passed through buffer IC3, and the gain is changed at the same level where the white balance is adjusted. In the AUTO white balance mode, the signal at pin 24 on the PR-72 board should be set to high.

5-9. Clamp Circuit

Gamma correction, white clip, and pedestal addition are performed in the process circuit. In this case, the optical black portion should be used as a voltage reference. The clamp circuit DC-fixes the optical black portion.

5-10. Offset Control

A level difference occurs at R, G, and B optical black portions in circuits of Step 5-11 and later steps, so it is adjusted to the G optical black level using R and B offset controls.

5-11. Multiplex (MPX)

R and B signals are sent every one H based on a linear sequential system. Therefore, respective signals passed through R and G channels by multiplexing are switched and joined using an ID pulse (inverted every one H).

5-12. Blanking Mix

Pre-blanking is performed during the H blanking period to clean and process the blanking portion.

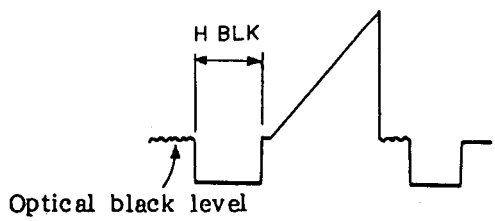


Fig. 5-12-1

5-13. γ Correction

γ correction is done so that the relationship between light input to a camera and light output from a photosensing screen is linear (γ = 1). The CCD's γ characteristics are γ1 = 1 and the CRT's γ characteristics are γ3 = 2.2, so γ2 = 0.45 is required in the electric circuit.

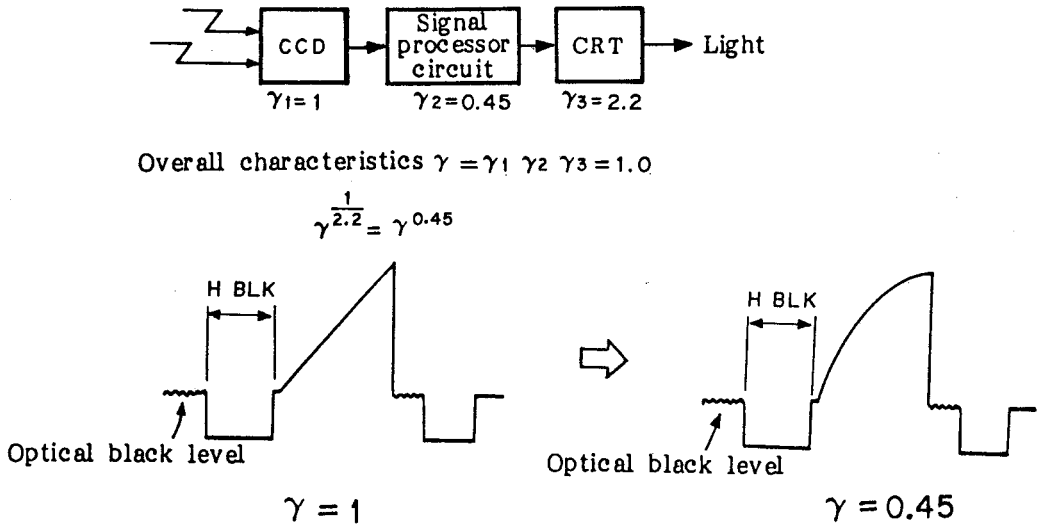


Fig. 5-13-1

5-14. White clip

When an image is shot at the white peak level, the level of white-balanced R, G, and B signals is increased. Therefore, when a signal exceeding a certain level is input, the white clip circuit clips the signal level and prevents it from exceeding the dynamic range of the next-stage circuit.

5-15. Pedestal Level

The luminance at a black level is determined by adding a DC level to the optical black level.

6. MD-30

6-1. Outline

GY and R/BY signals are input from the PR-72 board to a matrix circuit on the MD-30 board to produce YH, YL-YH, R-Y, and B-Y signals. The resultant signals are fed to an encoder circuit on the EN-40 board.

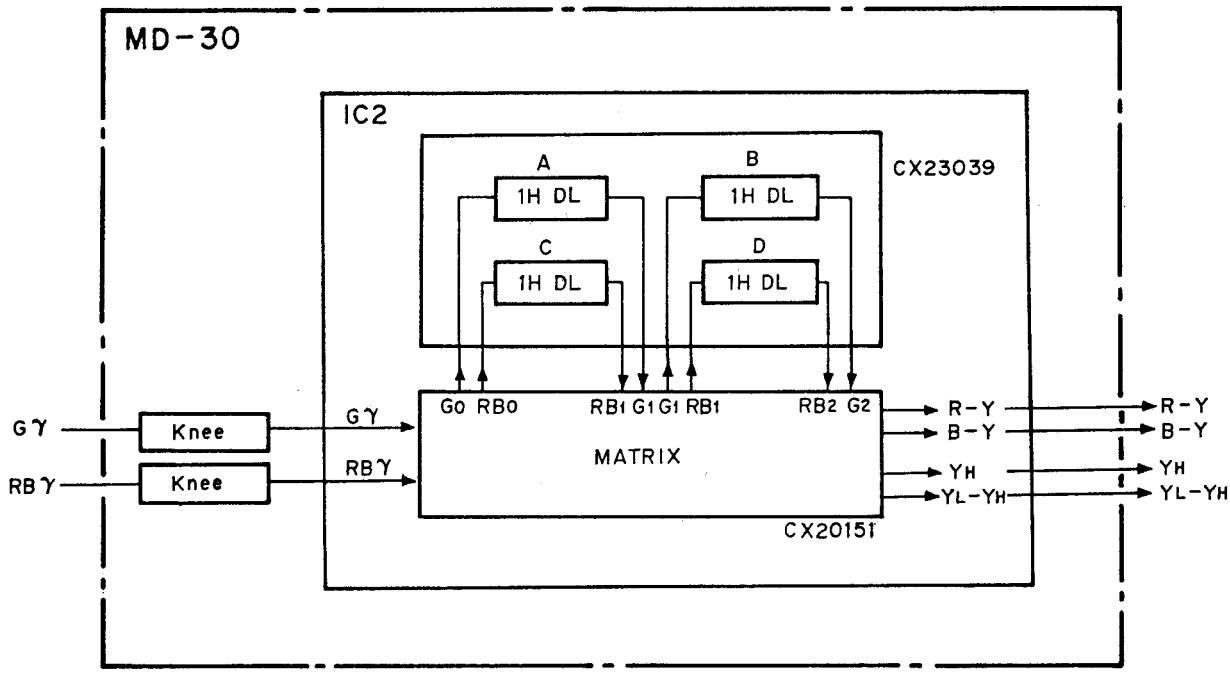


Fig. 6-1-1

. CX20151

In a color video camera employing a G-vertical stripe and R/G linear sequential system, when G and R/B signals are input and a 1H-delay line is connected, Y signals YH and YL-YH and color-difference signals R-Y and B-Y are output.

. CX23039

CX23039 is a CMOS CCD 1H-delay line used to process a linear sequential signal from the CCD camera. It has the following features:

(1) Internal clock drive circuit.

(2) Optimum bias can be automatically adjusted using an AUTO bias circuit (no adjustment is required).

(3) Four 1H-CCD delay lines.

(4) Pedestal clamp circuit.

6-2. Combination of CX23039 (CCD 1H-delay line) and CX20151

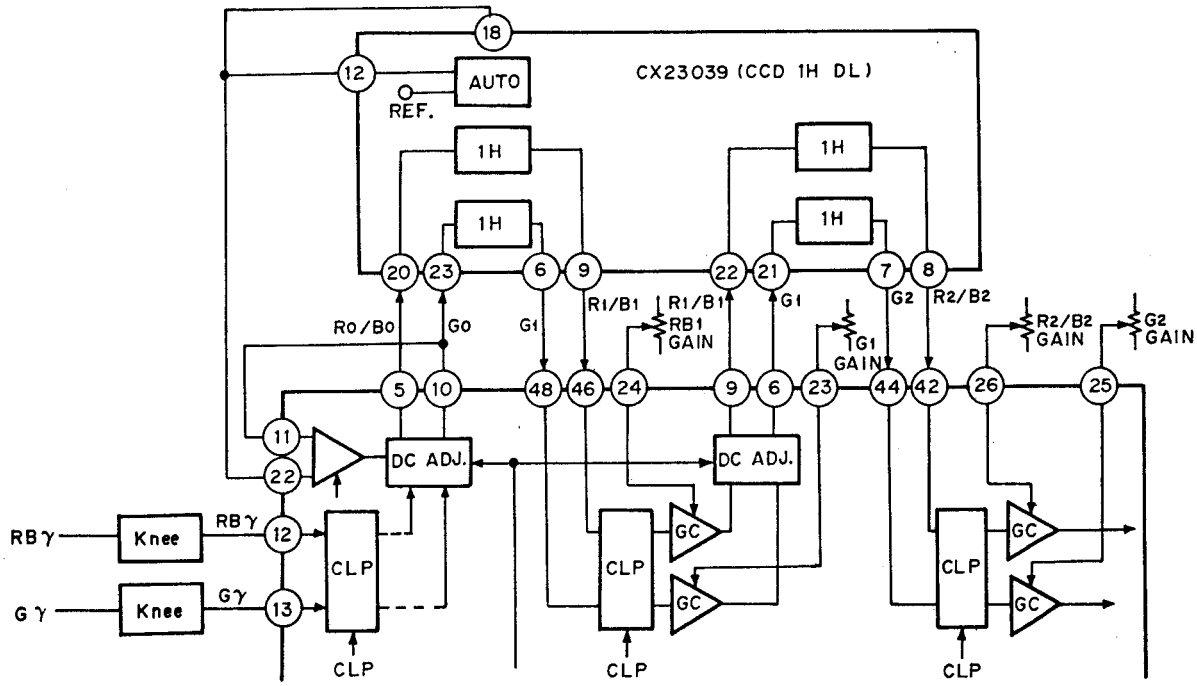


Fig. 6-2-1 CX20151

6-3. Knee Circuit

Knee circuits are provided in front of the CX20151 input stage to limit the signal dynamic range.

The characteristics are shown below.

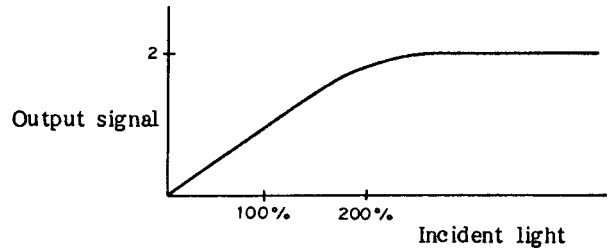


Fig. 6-3-1

The Gγ and R/Bγ signals sent to CX20151 are input to the clamp circuit and biased to an input potential required for a 1H-delay line (CX23039) by a DC adjuster circuit. The resultant signal is input to CX20151 as G0 and G0/B0 signals.

The G1 and R1B1 output signals passed through a 1H-delay line (one time) are clamped and DC-adjusted again using CX20151 and fed to the 1H-delay line (two times) to output G2 and R2B2 signals. As a result, G0, R0B0, G1, R1B1, G2, and R2B2 signals are produced.

6-4. CX20151 (Matrix)

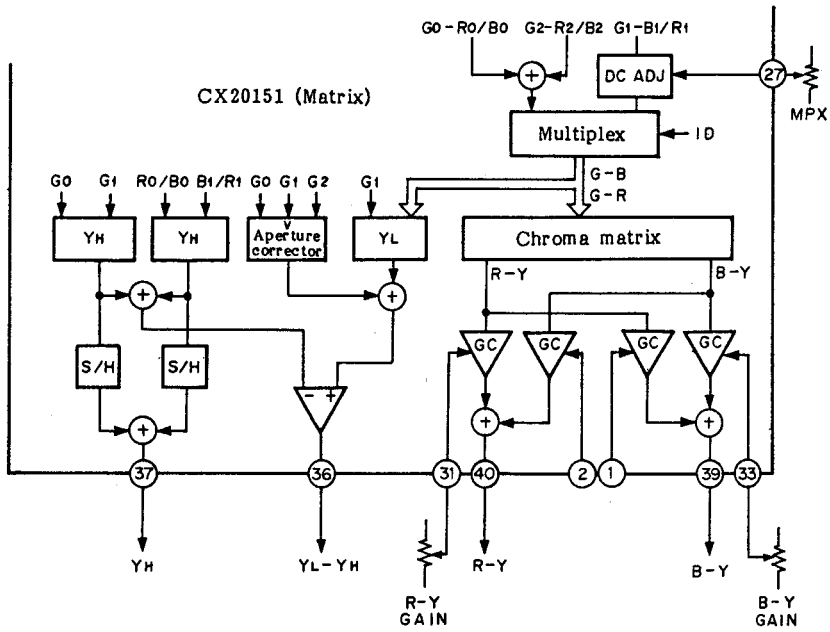


Fig. 6-4-1

Using G0, R0B0, G1, R1B1, G2, and R2B2 which are produced through the combination of CX20151 and CX23039, the desired signal is produced by YH, YLYH, R-Y, and B-Y signals from encoders.

. Aperture correction

The vertical aperture circuit is provided to sharpen the signal edge in the vertical direction.

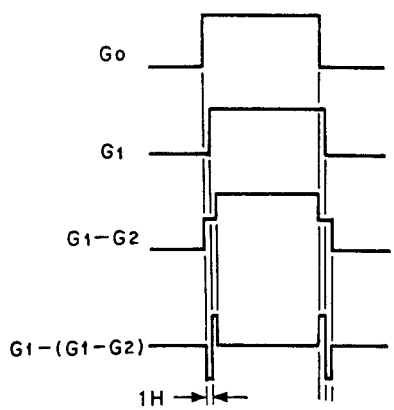


Fig. 6-4-2

6-5. CX23039 (1H-Delay Line)

When CX23039 is used combined with ICX018 (CCD), the input data rate is 4.77MHz and the delay time is as described below.

$T = 1/4.77 \times 301.5 \fallingdotseq 63.21\mu sec$

For an NTSC system, 1H is 63.55µsec (slightly short for 1H). Therefore, adjustment is made by extending only the last period of crystal delay lines XDL1 and XDL2. Using this system, a delay line can be used in common for PAL and NTSC systems.

6-6. Signal Processing Based on G-Vertical stripe, R/B Linear Sequential System

The CCD color filter is based on a G-vertical stripe, R/B linear sequential system, so a signal not containing blue and red signals is produced every one H. Therefore, the chroma signal not contained in line 1 must be compensated by adding 0-line and 2-line half signals using a 1H-delay line. For the B & W screen shown in Fig. 6-6-1, however, line 1 and line 2 are colored (misregistration) because of G-R $\neq$ 0 and G-B $\neq$ 0. To prevent the misregistration, the Y signal must be configured to meet the Y composition ratio conforming to an NTSC system.

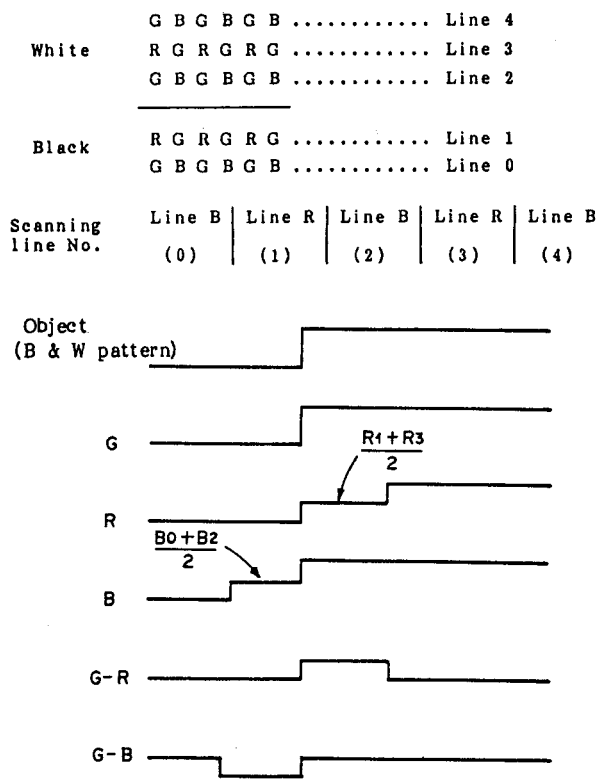


Fig. 6-6-1

G-B and G-R signals are then formed to produce Y and chroma signals. The color-difference signals in the NTSC system are as follows:

$$R\text{-}Y = R - (0.59G + 0.3R + 0.11B)$$
$$= 0.11\,(G - B) - 0.7\,(G - R)$$
$$B\text{-}Y = B - (0.59G + 0.3R + 0.11B)$$
$$= 0.3\,(G - R) - 0.89\,(G - B)$$

The color-difference signals described below are obtained using a matrix.

. When a line (1 line) is GR

$$R\text{-}Y = 0.1 \times 1/2\,\{(G0 + G2) - (B0 + B2)\} - 0.7\,(G1 - R1)$$
$$B\text{-}Y = 0.3\,(G1 - R1) - 0.9 \times 1/2\,\{(G0 + G2) - (B0 + B2)\}$$

. When a line (1 line) is GB

$$R\text{-}Y = 0.1\,(G1 - B1) - 0.7 \times 1/2\,\{(G0 + G2) - (R0 + R2)\}$$
$$B\text{-}Y = 0.3 \times 1/2\,\{(G0 + G2) - (R0 + R2)\} - 0.9\,(G1 - B1)$$

This prevents misregistration.

The Y signal in the NTSC system is as follows:

$$Y = 0.59G + 0.3R + 0.11B$$
$$= 0.11\,(B - G) + 0.3\,(R - G) + G$$

The Y signal described below is obtained using a matrix.

. When a line (1 line) is GR

$$YL = 0.11 \times 1/2\,\{(B0 - G2) - (G0 + G2)\} + 0.3\,(R1 - G1) + G1$$

. When a line (1 line) is GB

$$YL = 0.11\,(B1 - G1) + 0.3 \times 1/2\,\{(R0 + R2) - (G0 + G2)\} + G1$$

where the Y signal described previously is prescribed as YL.

YL consists of G0, G1, G2, RB0, RB1, and RB2. The resultant sampled frequency is 4.77MHz (SP1, SP2). The frequency range of the CCD output is more than 4.77MHz, so YL is equal to G1 (YL = G1) when a B & W object is shot. As a result, reflected distortion occurs as shown in Fig. 6-6-2.

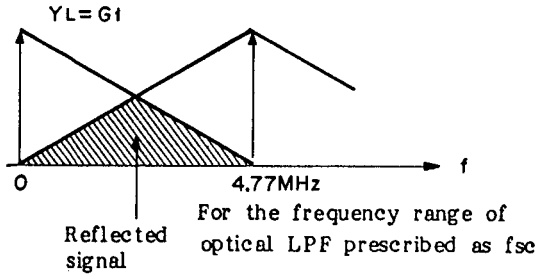


Fig. 6-6-2

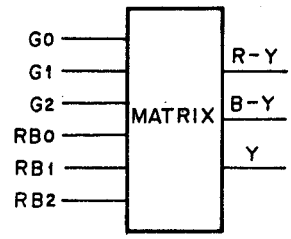


Fig. 6-6-3

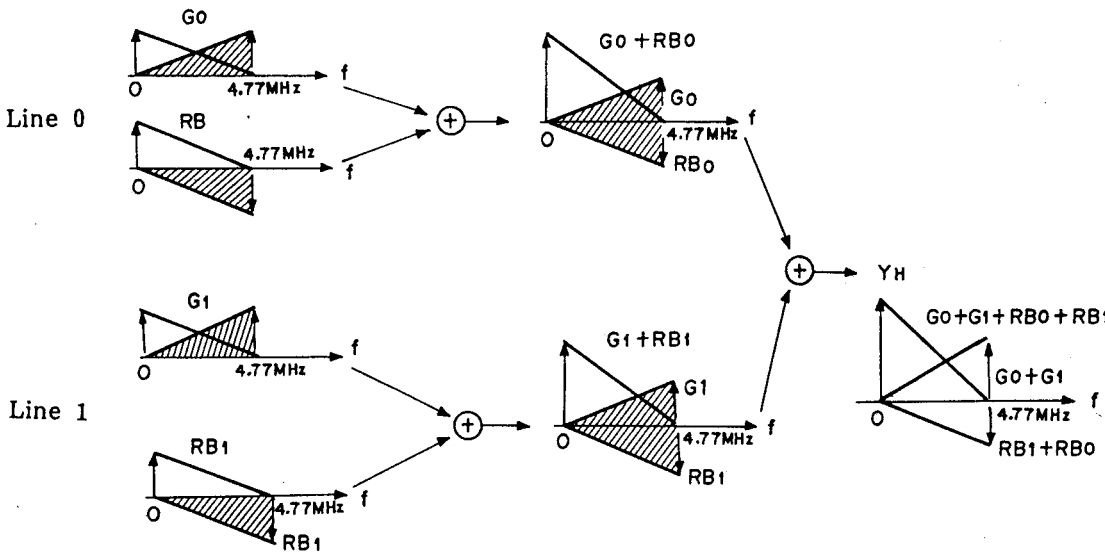


Fig. 6-6-4

When a frequency range exceeding 1/2 x 4.77MHz is sampled using a 4.77MHz frequency, reflected distortion occurs (sampling theorem). To eliminate the resultant reflected signal, G1 and RB1 signals, which are shifted by 180 degrees compared with G0 and RB1 signals shown in Fig. 6-6-4, are added to produce a YH signal. As a result, each B & W image is canceled and no reflected distortion occurs. The YH signal is configured using a matrix as follows:

. When a line (1 line) is GR

$YH = 0.25 (G0 + G1) + 0.25R1 + 0.25B0$

. When a line (1 line) is GB

$YH = 0.25 (G0 + G1) + 0.25R0 + 0.25B1$

The composition of the YH signal is 0.5 : 0.25 : 0.25 = G : R : B, which differs in composition ratio from the Y signal in the NTSC system.

Y signals outside the 0.5MHz chroma range appear natural even at the composition ratio described above. For the Y signal not exceeding the 0.5MHz chroma range, however, the ratio of G, R, and B signals in the NTSC system must be 0.59 : 0.3 : 0.11. Therefore, in the low-frequency range the YL signal is produced based on an NTSC composition ratio. In the high-frequency range, the Y component of the YH signal is produced to compensate for the reflected distortion. The boundary line between the low and high-frequency ranges is approximately 0.7MHz in this system. When the YL and YH signals are composed, the signal produced when YL - YH (obtained by subtracting YH from YL) and YH are added is prescribed as a Y signal.

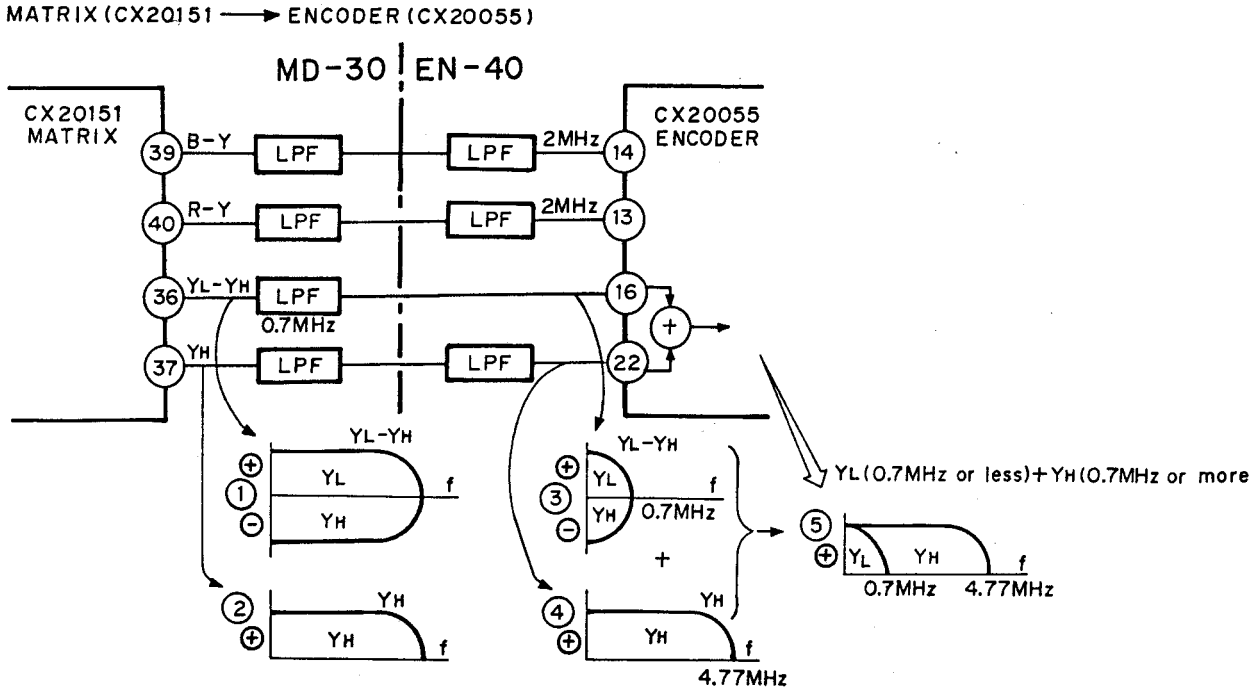


Fig. 6-6-5

YL - YH is indicated by (1) and YH by (2) in Fig. 6-6-5. YL - YH (1) passes through a low-pass filter and becomes (3). YH (2) passes through low-pass filters consisting of two stages and becomes (4). When (3) and (4) are added using an encoder IC on the EN-40 board, (5) is produced.

Vertical correlation processing

1. Color-difference signals

R - Y = 0.7R - 0.6G - 0.1B
B - Y = 0.9B - 0.6G - 0.3R
⟵ Three-line correlation
Configured by G1 - R1/B1, 1/2 {(G0 - B0/R0) + (G2 - B2/R2)}.

2. Y signals

YL = 0.59G + 0.3R + 0.11B ⟵ Three-line correlation
Configured by G1 - R1/B1, 1/2 {(G0 - B0/R0) + (G2 - B2/R2)}, G1.

YH = 0.5G + 0.25R + 0.25B ⟵ Two-line correlation
Configured by G0, G1, R0/B0, B1/R1.

Line 0	G0	R0	G0	R0
Line 1	G1	B1	G1	B1
Line 2	G2	R2	G2	R2

G stripe R/B linear sequence

Fig. 6-6-6

The waveforms obtained when a pattern box is shot are shown below.

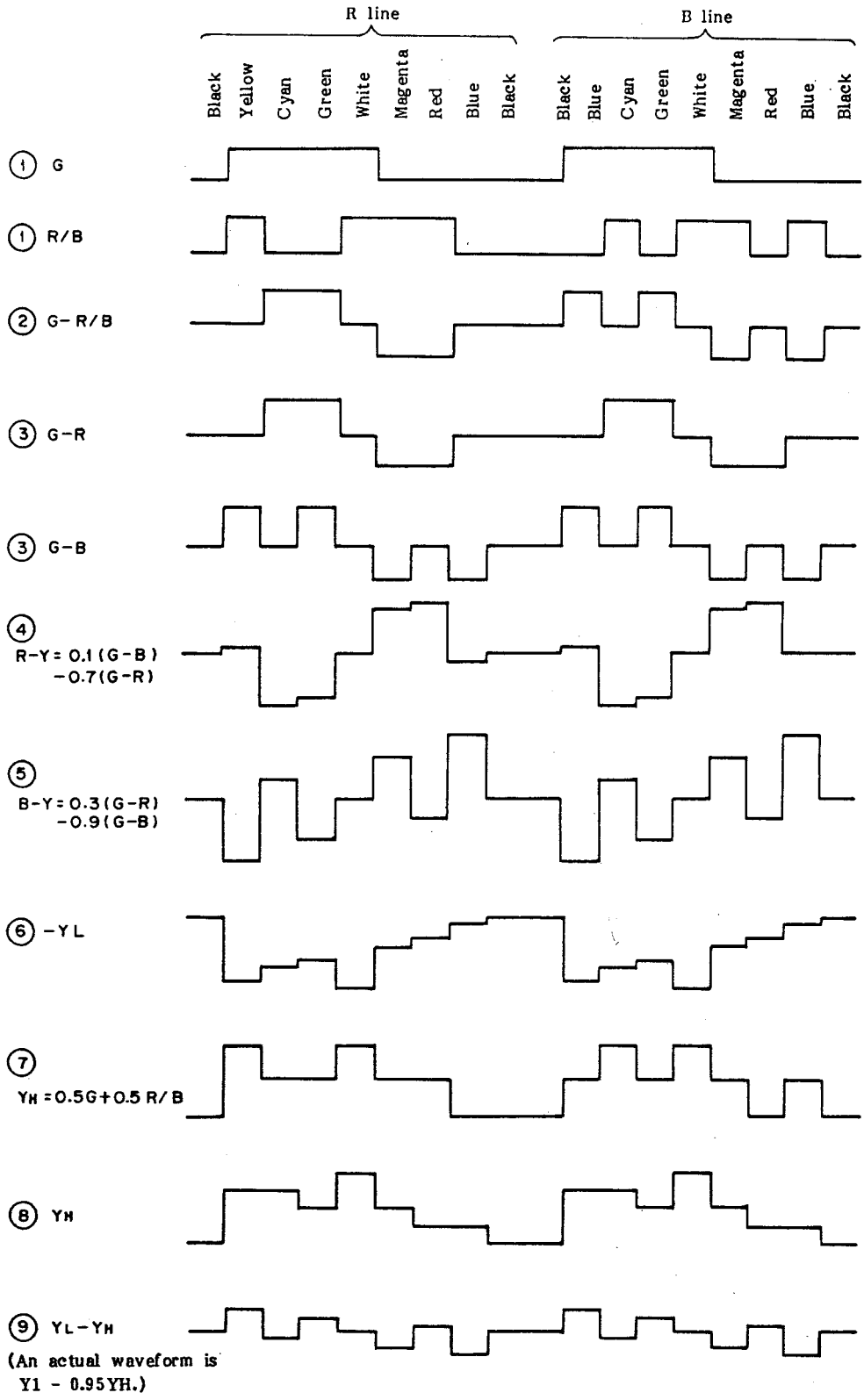


Fig. 6-6-7

7. EN-40

7-1. Outline

Output signals YH, YL-YH, R-Y, and B-Y from the MD-30 board are input to the EN-40 board to process Y and chroma signals and output from the EN-40 board as a video signal. B & W signals and color-difference signals are also output through a buffer.

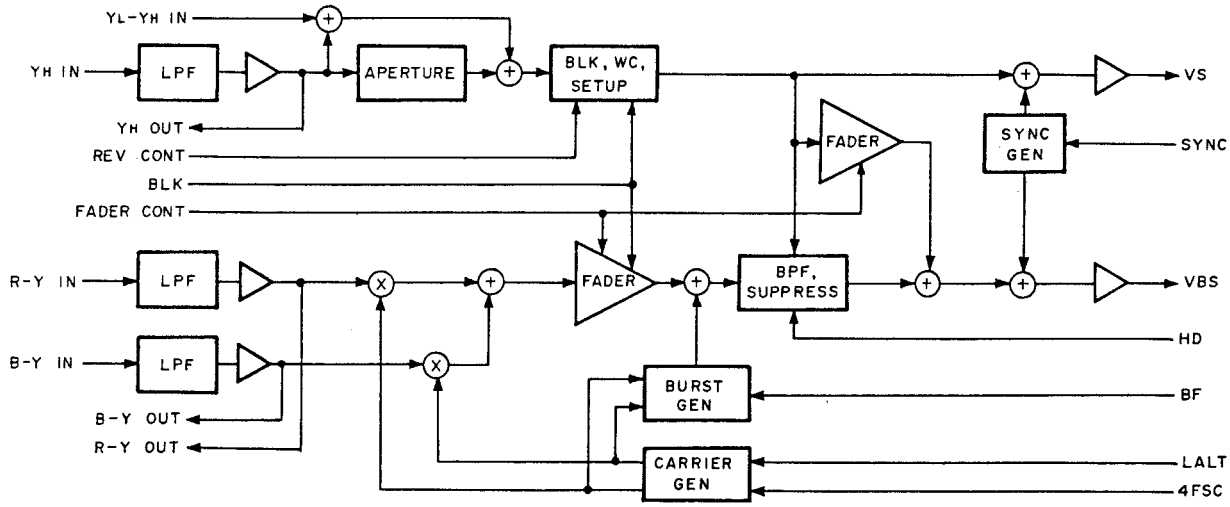


Fig. 7-1-1 EN-40 Board Block Diagram

Output signals YH, R-Y, and B-Y from the MD-30 board are output from a camera through a buffer.

7-2. Y Signal Processing

Signals YH and YL-YH from a matrix IC (CX20151) are sent to pins 16 and 22 of IC2 (CX20055).

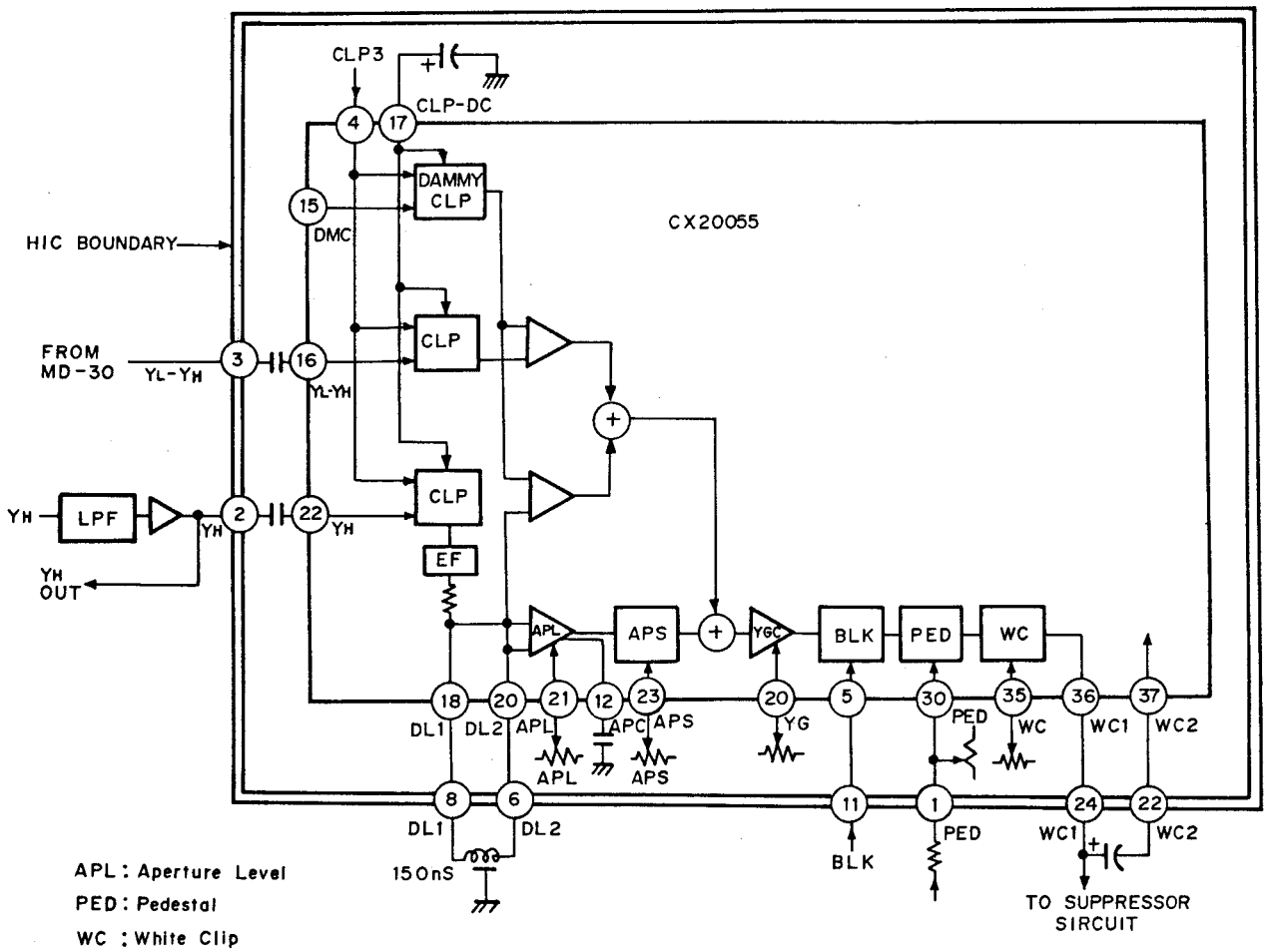


Fig. 7-2-1

7-3. Clamp Circuit

The YH and YL-YH signals which are input to pins 16 and 22 of IC2 are clamped during the H blanking period. This clamp circuit also produces the DC level required for processing the resultant signals by using a differential amplifier (dummy clamping).

7-4. Aperture Correction

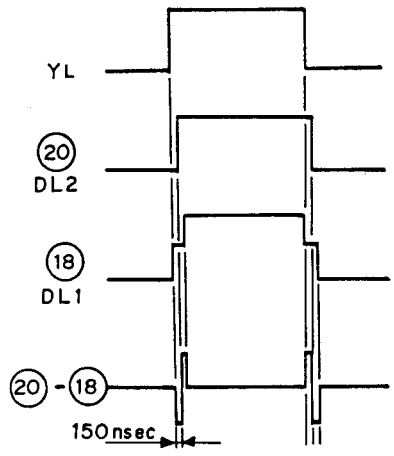


Fig. 7-4-1

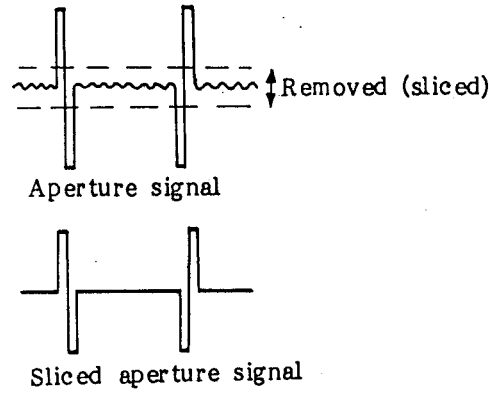


Fig. 7-4-2

The YH signal is sent to a delay line at an output impedance of 1k ohm (the delay time is 150msec). The delay line is terminated at a high impedance. Therefore, a reflected wave occurs and is added to the YH signal at pin 18. The signals at pins 18 and 20 are fed to a differential amplifier to produce an aperture signal.

The gain is set at a 21-pin APL terminal. The low-level component of the aperture signal which is generated at the APL block is eliminated at an APS block. To eliminate the noise component amplified at the APL block, the slice level is set at a 23-pin APS terminal.

The Y signal consisting of YH and YL-YH is also formed with the aperture signal.

The aperture correction is performed in the horizontal direction.

7-5. YG, PED, and WC Terminals

After the Y signal amplitude is adjusted at a 29-pin YG terminal, the blanking level is blanked and appropriately clipped at a 30-pin PDE terminal to obtain a pedestal level. The signal at the PED terminal is output to the camera terminal through a resistor and can be controlled by supplying 0 to 5V dc from the external unit. White clipping is done at a 31-pin WC terminal.

7-6. Y, Sync, and Chroma Signal Mixing

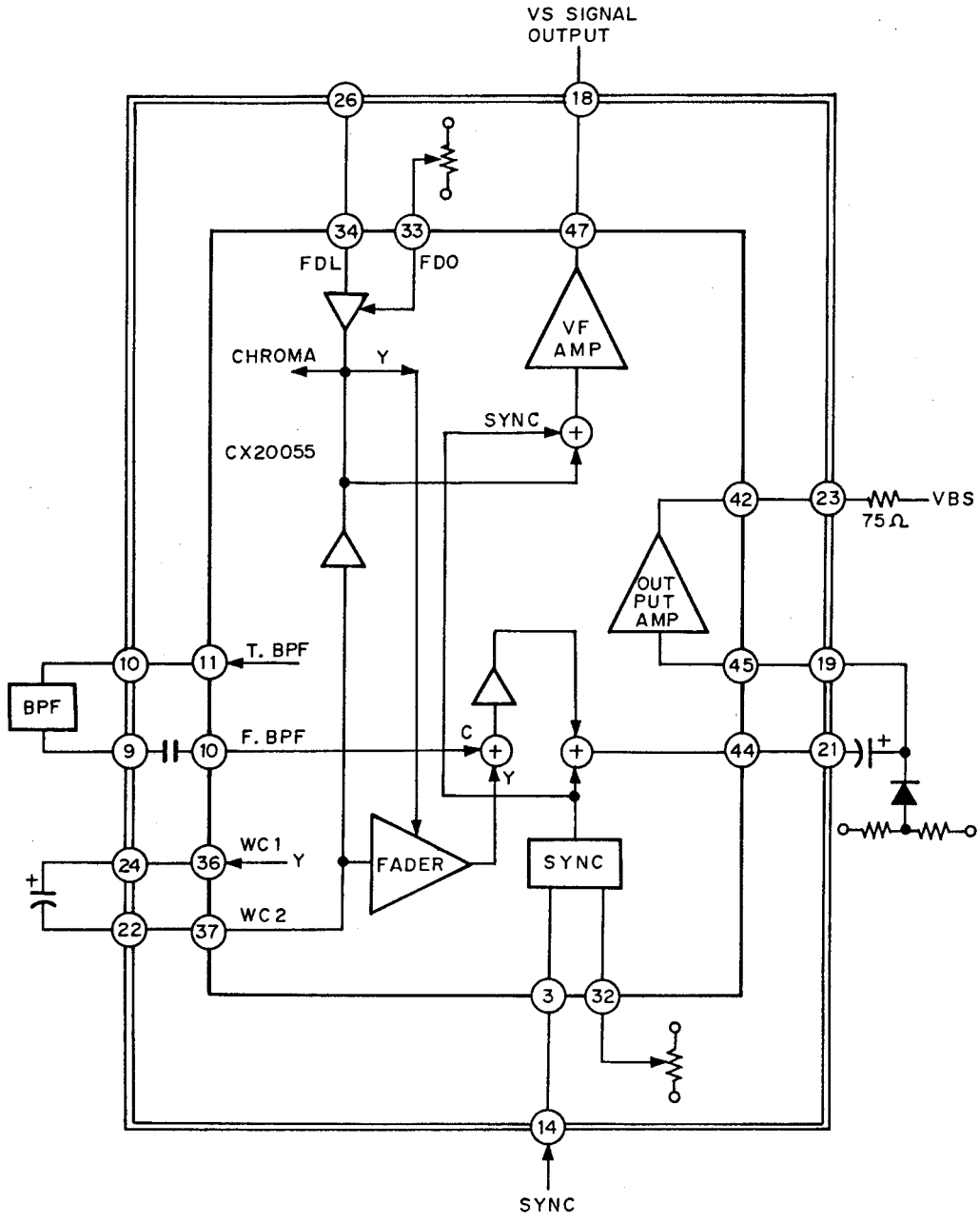


Fig. 7-6-1

As shown in Fig. 7-6-1, the white-clipped Y signal is output from pin 36 of CX20055 and sent through a capacitor to pin 37. The chroma signal is output from pin 11 of CX20055 and sent through a band-pass filter to the F.BPF terminal at pin 10 to form the Y signal and chroma signal. After that, a sync signal is added and output from pin 44. The final signal is output from pin 42.

7-7. VS Signal Output

The VS signal which is a B & W signal with a sync signal is output for AUTO iris adjustment. A fader function (described in Step 7-8) is not activated for this signal. To make the AUTO iris adjustment by using this signal, a special lens is required. The output resistance is not 75 ohms, so the VS signal cannot be supplied to a TV monitor.

7-8. Fader

When the voltage at pin A15 is changed, the fader function is activated for a VBS signal.

7-9. Chroma Signal Processing

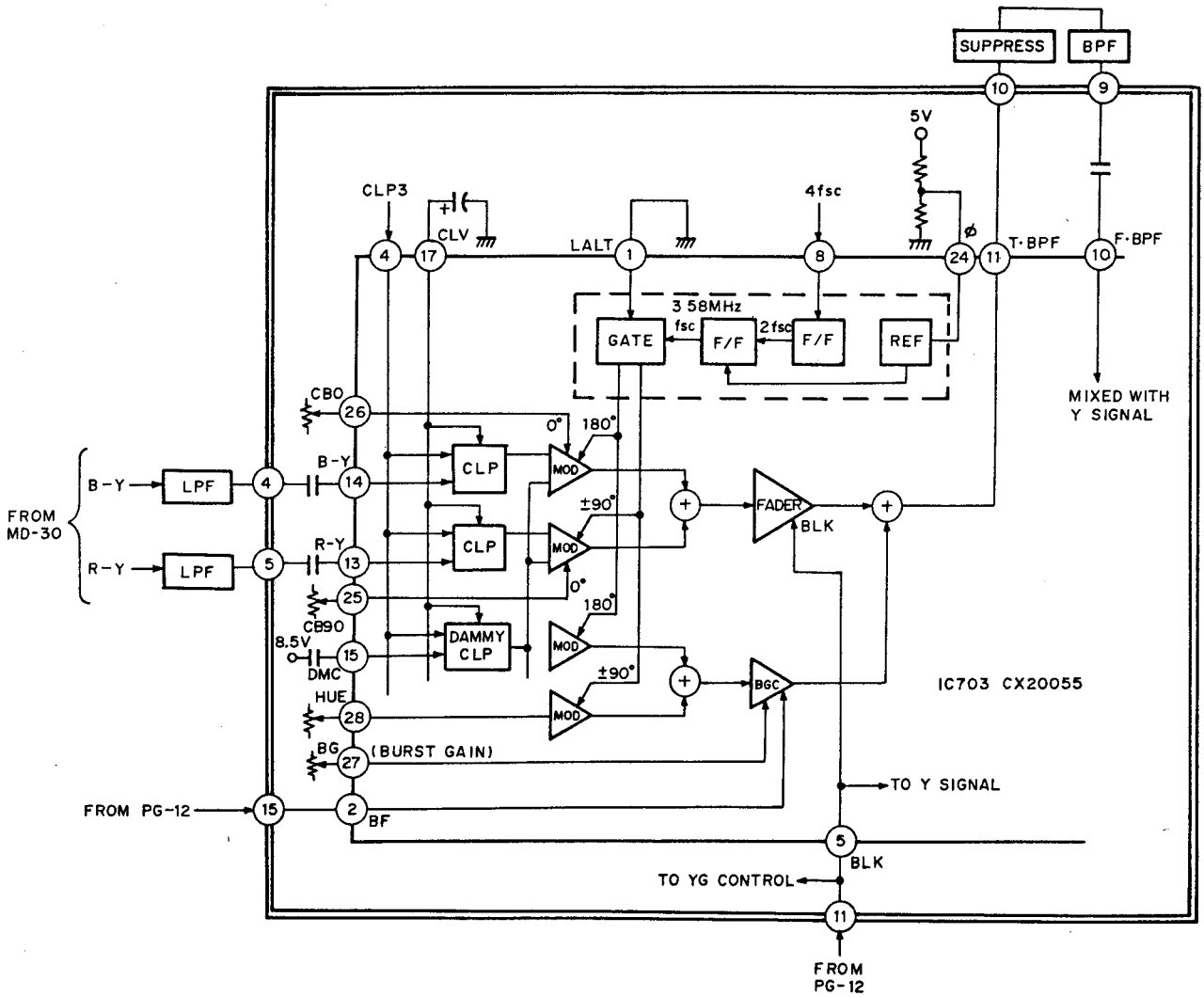


Fig. 7-9-1 Chroma Signal Processing of CX20055

7-10. Quadrature Chroma Subcarrier Generation

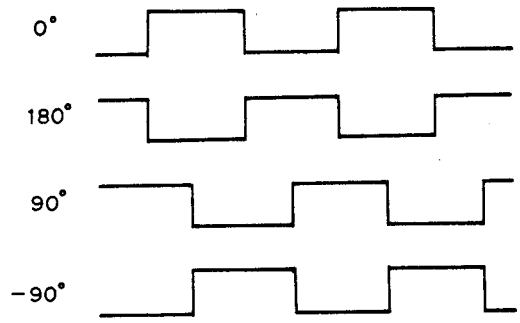


Fig. 7-10-1

The 4fc (14MHz) signal at pin 8 is frequency-divided into fsc using a flip-flop to produce 0° and ±90° subcarriers. At that time, 0° and ±90° phases are adjusted using set voltage ø at pin 24.

In the gate circuit, 0°, 180°, 90°, and -90° component subcarriers are formed at 0.35V using the ECL-level (0.7V) subcarriers (0° and ±90°) from the former stage. When the gate is closed or opened using the H ALT signal (TTL-level) at pin 1 every one H, the polarity of 90° and -90° components can be selected to accommodate a PAL system.

7-11. Color Burst Signal Generation

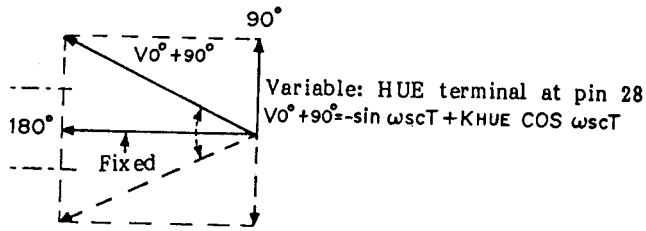


Fig. 7-11-1

The gain of the 0° component subcarrier from the gate is fixed, and a vector is formed with the 90° component as a variable gain. The resultant component is extracted using a burst flag pulse (BF at pin 2) from the external unit, and the gain is adjusted using set voltage BG at pin 17.

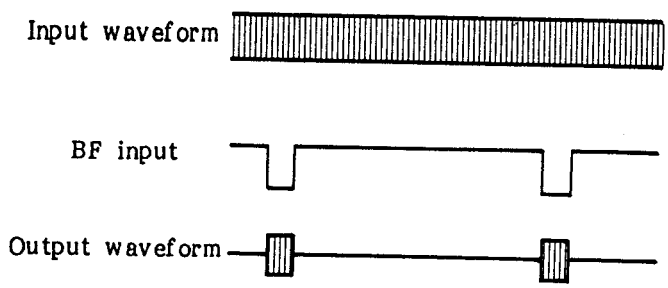


Fig. 7-11-2

7-12. Modulator Circuit

Color-difference signals R-Y and B-Y from the MD-30 board are passed through a low-pass filter and input to pins 13 and 14 of CX20055. The resultant R-Y and B-Y signals are clamped during the H blanking period and modulated using 90° and 0° component subcarriers.

The offset which occurs in a clamp circuit can be compensated using CB90 at pin 25 and CB0 at pin 26. At that time, the carrier leakage during B & W shooting can also be suppressed.

The modulated R-Y and B-Y signals are combined to produce composite output Vo.

$$Vo = KRVR - Y \ Sin\omega sct - KBVB - YCos\omega sct$$

7-13. Burst Mix Circuit

The subcarrier signal blanked using a burst flag signal is input to a burst gain control circuit, where the burst level is adjusted using a volume control (not mounted on the board) at pin 27. The burst flag signal is mixed with a modulated chroma signal, output from pin 11, and passed through a chroma suppressor circuit. The resultant output is then band-limited using a band-pass filter, input to pin 10 again, and mixed with a Y signal.

7-14. Chroma Suppressor Circuit

The chroma suppressor circuit is used to attenuate the chroma signal so that a Y signal is not colored when it is saturated.

The Y signal which is white-clipped at pin 7 of IC1 through Q7, Q4, and Q8 is input with a positive polarity. The modulated chroma signal is input to pin 5.

When the Y signal is saturated with the DC potential at pin 1 adjusted to the Y signal's white-clip level, no chroma signal is output because opposite-phase and in-phase chroma signals passed through Q2 and Q4 cancel each other. The output of the band-pass filter is attenuated using Q5 and Q6 only when a horizontal driving pulse is low.

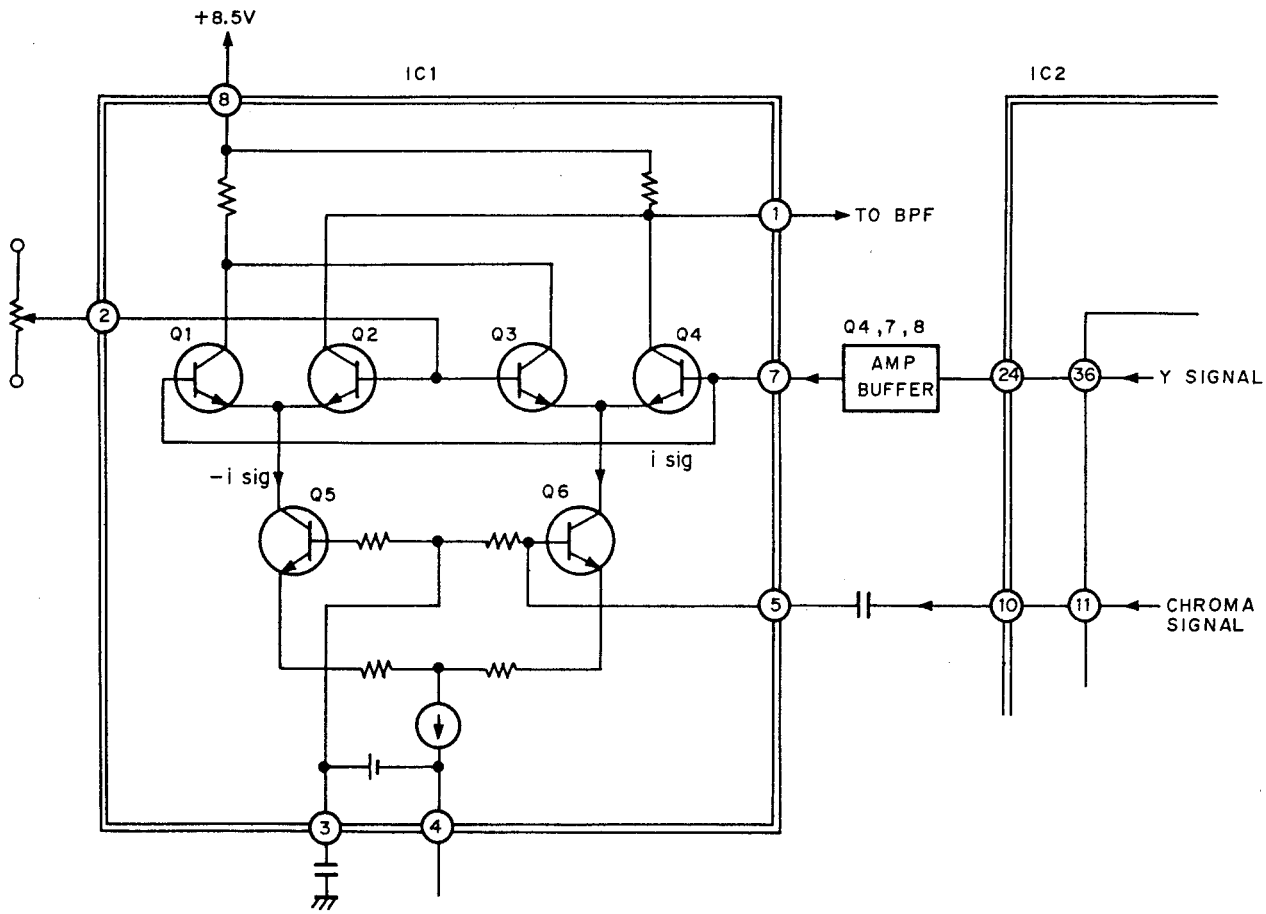


Fig. 7-14-1

8. RG-13

8-1. Outline

The RG-13 board consists of a switching circuit to select the 4fs required for chroma signal modulation and VCO control voltage on the PG-12 board using an external sync/internal sync system; a +12V regulated voltage generator circuit; an auto white balance backup capacitor; and a smoothing circuit with 20V, 8.5V, and +5V power supplies.

. NTSC

When the signal at pin 22 on the RG-13 board is low, pin 5 of IC1 (3/3) is selected. The voltage adjusted using RV2 is input from pin 21 to the PG-12 board and applied to a 4fc VCO. The resultant frequency is used as a basic clock for cameras. Using the 4fc, a horizontal scanning frequency is also produced in the PS-12 board.

. PAL

When the signal at pin 22 on the RG-13 board is low, pin 2 of IC1 (2/3) is selected. The voltage adjusted using RV2 is input to VCO 1 to generate a 4fc frequency. The resultant frequency is used as a subcarrier signal for cameras. To lock a horizontal scanning frequency to the subcarrier in the PAL system, a horizontal control voltage is input from the PG-12 board to pin 23 on the RG-13 board and output from pin 21 on the RG-13 board through buffer Q3, operating the VCO on the PG-12 board.

8-2. Internal/External Sync Selection

. NTSC

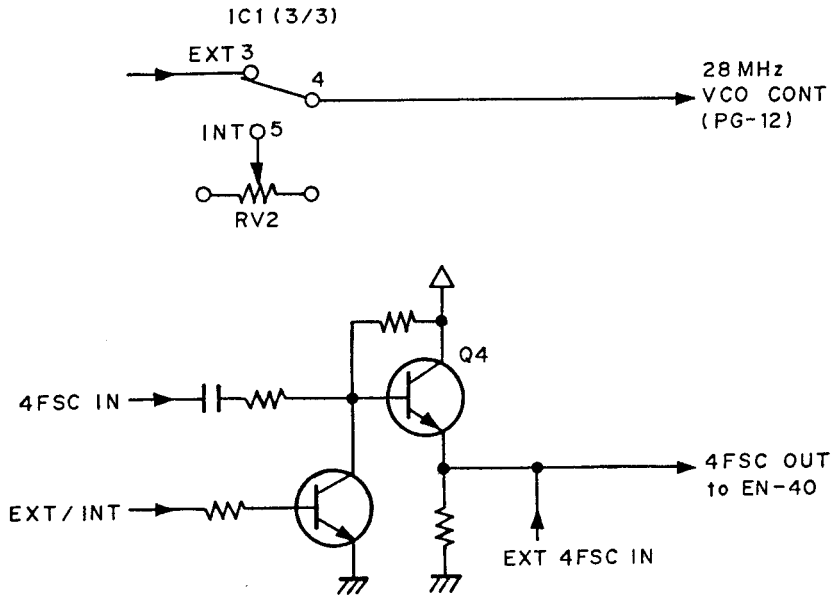


Fig. 8-2-1

Only the switch consisting of pins 3, 4, and 5 in IC1 is used.
For internal sync, the switch consisting of pins 4 and 5 is turned on, and the voltage adjusted using RV2 is input from pin 21 to the PG-12 board, causing a 28MHz VCO to oscillate. Q5 is turned off, so Q4 functions as a buffer. The 4fsc frequency which is input from the PG-12 board to pin 30 is sent to the EN-40 board using Q4. For external sync, the switch consisting of pins 3 and 4 is turned on, and the SC COM voltage which is input from the external unit to pin 25 is sent to VCO. Q5 is turned on and Q4 is turned off. At that time, no 4fsc frequency is output from the PG-12 board.

. PAL

The switch consisting of pins 3, 4, and 5 in IC1 is not used.
For internal sync, the switch consisting of pins 3, 4, and 5 is turned on, and the voltage adjusted using RV2 is input to VCO to produce a 4fsc pulse. The pulse is fed to the PG-12 board as a reference signal to lock the signal generator's clock frequency. The switch consisting of pins 12 and 14 is then turned on, so the H COM voltage from the PG-12 board is fed to a 28MHz VCO. Moreover, Q5 is turned off. Therefore, Q4 functions as a buffer and sends a 4fsc pulse to the EN-40 board.

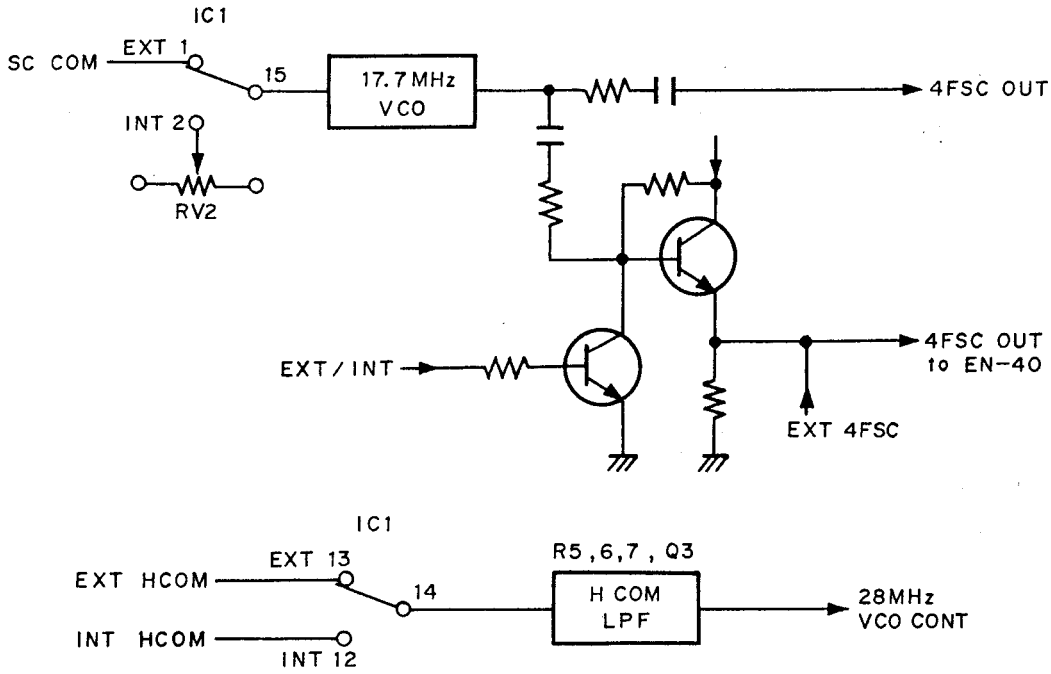


Fig. 8-2-2

For external sync, the switches consisting of pins 1 and 15, and pins 13 and 14 are turned on. Therefore, the SC COM and EXT H COM voltages from the external unit are sent to 4fsc and 28MHz VCOs, respectively.

8-3. +12V Regulated Voltage Generator Circuit

The +20V from the MB-37 board is input to the +12V regulated voltage generator circuit consisting of Q1 and Q2. Therefore, +5V is input from the MB-37 board as a reference voltage and compared using IC2 to output a constant +12V voltage.

9. AT-40

9-1. Outline

The AT-40 board consists of the following circuits:

(1) AGC circuit (controlled from -6dB to +3dB)

(2) Auto white balance circuit

9-2. AGC Circuit

The AGC amplifier is controlled so that the signal level is 0dB in the AUTO mode.

The AGC detection signal is passed from pin 20 on the PR-72 board through pin 23 on the AT-40 board and sent to pin 12 of CX20056. The resultant signal is then clamped, amplified by 3.3 times, and output from pin 14 of CX20056. After that, the weighting signal generated from a vertical driving pulse is added and the resultant signal is output to an AGC detector circuit.

When the weighting signal is added, the portion corresponding to the upper area of the screen is not detected.

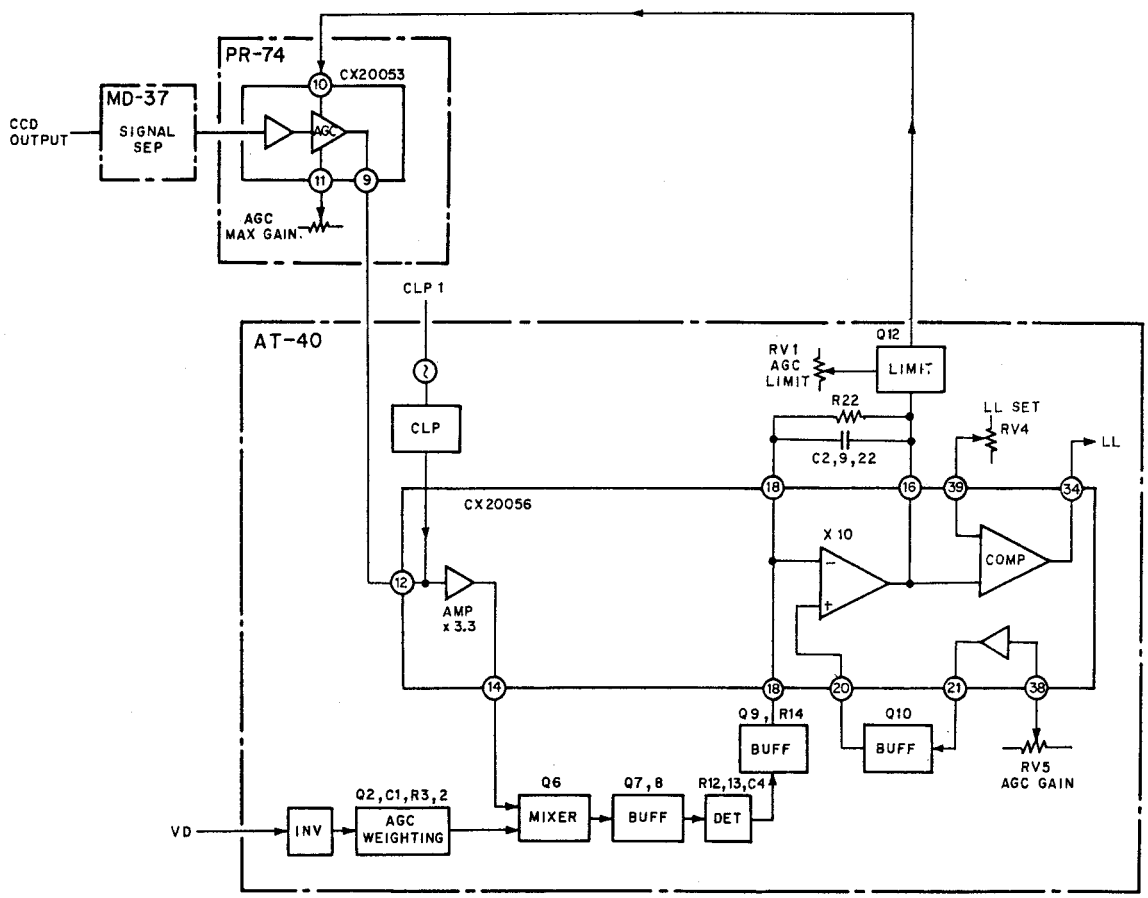


Fig. 9-2-1

The weighting signal generated from a vertical driving pulse is a V-period sawtooth wave of which tilt is determined by C1 and R3.

When the weighting signal is mixed with the AGC detection signal using Q6, the level at the upper area of the screen is weighted.

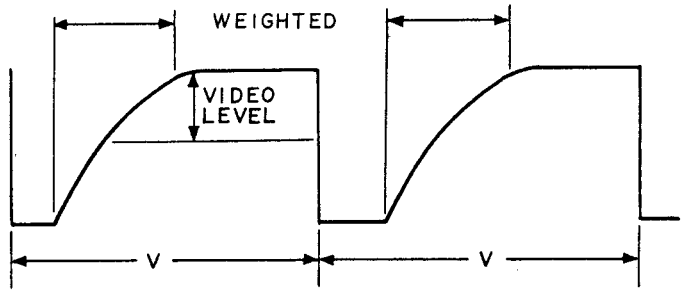


Fig. 9-2-2

The weighted detection signal is converted into a DC voltage using a detector circuit and input to pin 18 of CX20056. The input signal is then amplified by -10 times and output from pin 16. The output offset is adjusted using the voltage set by RV5.

The output voltage at pin 16 of CX20056 is limited using Q12 and RV1. At that time, the lower limit of the AGC amplifier gain is determined. The resultant voltage is 2 to 4V dc. The CX20053 amplifier gain is controlled in the range of -6dB to +3dB using the voltage.

CX20056 has a low-light detector circuit. When the AGC voltage exceeds the level set by RV4, the voltage at pin 34 goes low to inhibit the auto white balance trigger and prevents activation of the auto white balance circuit.

9-3. Auto White Balance Circuit

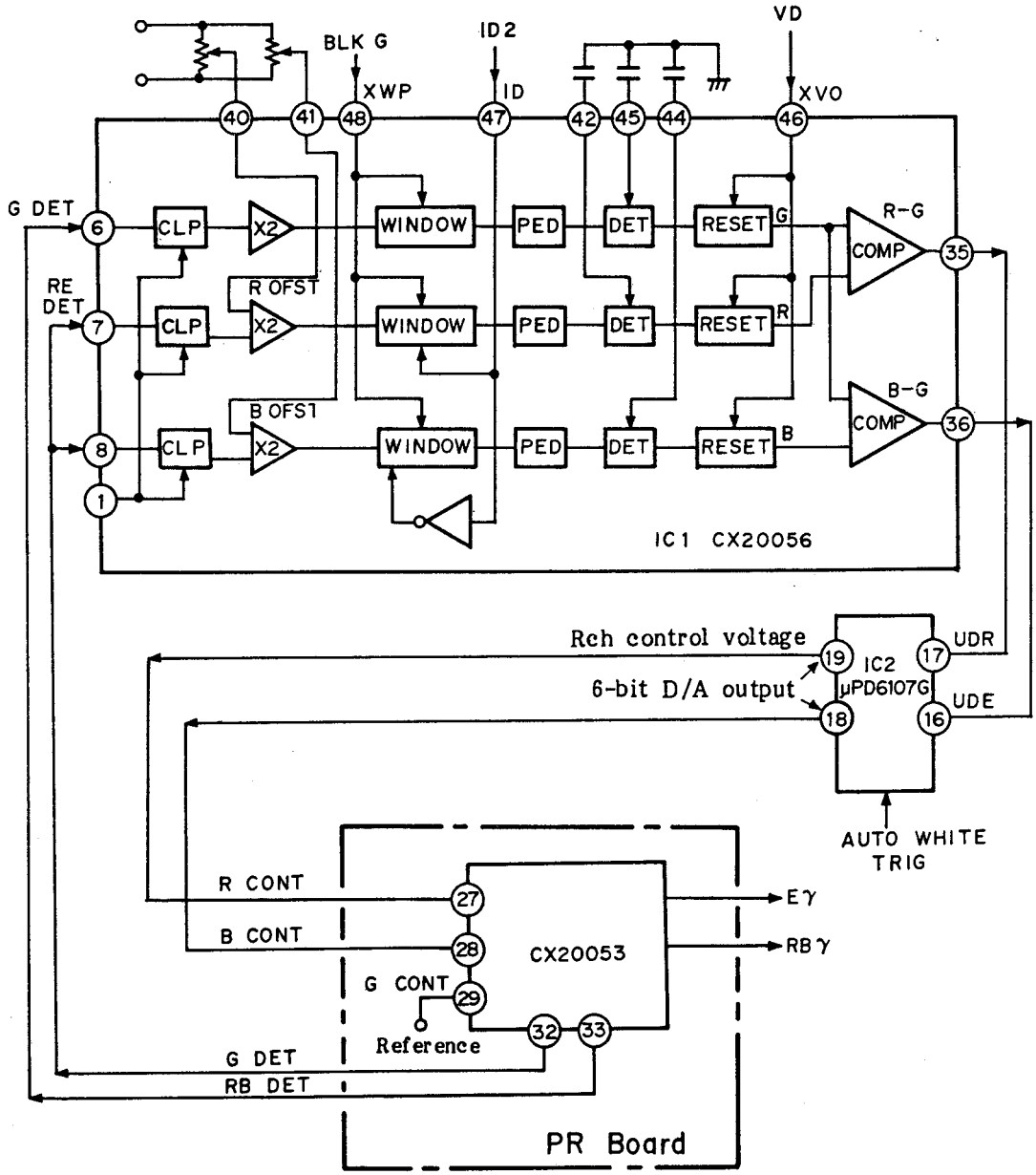


Fig. 9-3-1

Auto white balance adjustment is performed through the combination of CX20053 on the PR-72 board and CX20056 on the AT-40 board.

G DET and RG DET signals are input from CX20053 on the PR-72 board to CX20056 on the AT-40 board. The resultant input signal is then sent to a clamp circuit, passed through an amplifier with double the gain, and input to a widow circuit to gate it using a composite blanking signal. When the composite blanking signal is used, a picture appears on the whole display of the screen which is detected by a white detector circuit, where the R/B signal which is sent every one H using a 1D pulse is separated into a monochromatic signal. The resultant signal is then sent to a pedestal circuit and input to a peak detector circuit. A 3CH-peak voltage is detected using the peak detector circuit to compare the R-G and B-G signals. A low or high voltage is then output.

A vertical driving pulse is input from pin 46 of CX20056, and a charging voltage for peak detection is discharged every one volt for reset operation.

The output levels at pins 35 and 36 of CX20056 are as follows:

G > R/B High

G < R/B Low

The output voltage is attenuated, level-shifted, and input to CX20053 on the PR-72 board to adjust R and B signal gains to a G signal level.

9-4. IC2 μPD6107G Operation Theory

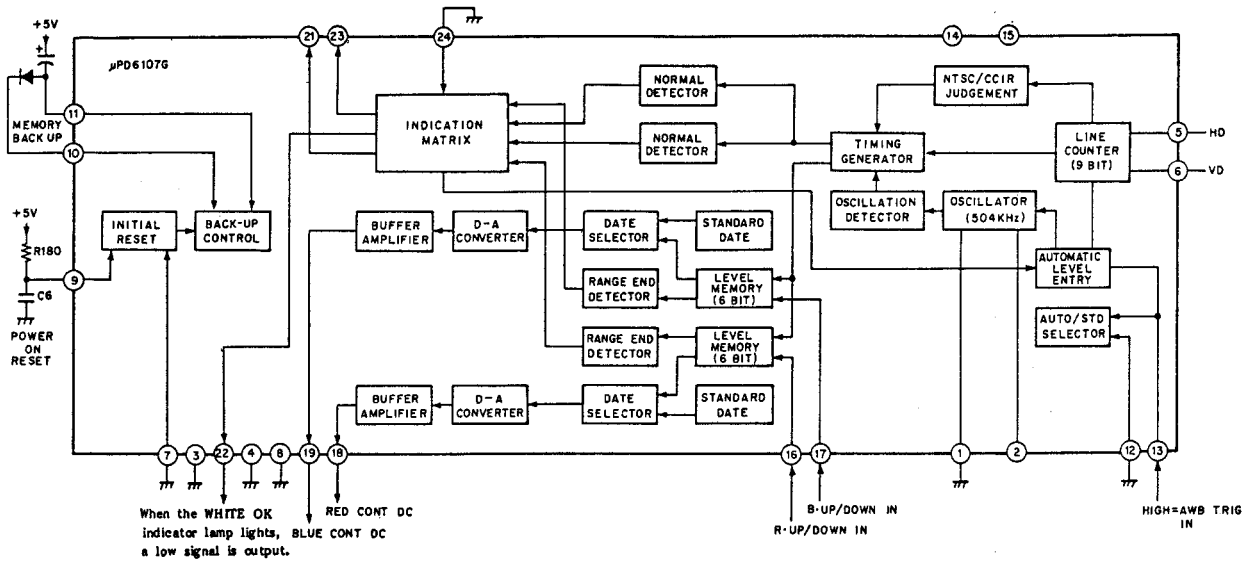


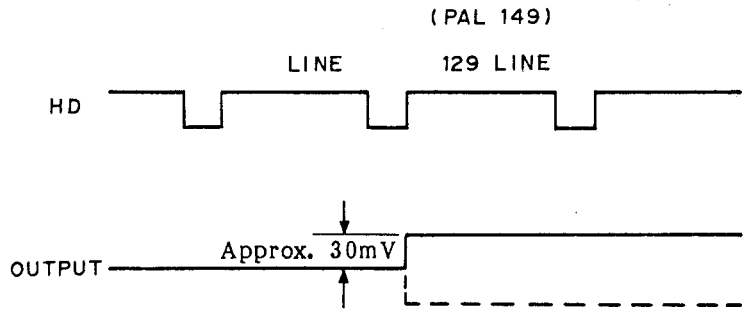
Fig. 9-4-1

Using IC2, the auto white balance control voltage is generated and data memory is stored.

A 6-bit counter is incremented or decremented using high and low signals at pins 17 and 16. The counted value is then D/A converted and output. The output voltage is 1.5V to 3.3V.

When a high signal is input to pin 13 of μPD6107G, operation is initiated. The 6-bit level memory data from pins 16 and 17 is incremented or decremented depending on whether comparison signals B-G and R-G of CX20056 are high or low. When 1-bit increment or decrement is performed, the voltages at pins 18 and 19 are changed by approximately 30mV. The increment or decrement is done bit by bit every one volt until an UP/DOWN signal is inverted. The point at which the UP/DOWN signal is inverted is prescribed as white balance data. The data is stored in the level memory and held using a backup capacitor on the RG-13 board (for two or three days).

Data output timing



1-bit increment or decrement

* The horizontal driving pulse is preset using a vertical driving pulse. For CCIR and NTSC, selection is automatic.

Fig. 9-4-2

After white balance adjustment is completed, a low signal is output from pin 22 of µPD61076. The output signal is used for a white balance indicator. In the low light mode, a signal to inhibit the white balance operation is output from pin 34 of IC1 CX20056. When the video level is less than 30%, the output signal goes high. At that time, Q15 and Q16 are turned on, and the signal at pin 13 of IC2 remains low to cancel the auto white balance trigger.

10. PG-12

10-1. Outline

The PG-12 board contains a pulse generator with an external GENLOCK and internal signal generator. To establish the external synchronization, CL, SC, and FH pulses are output to the external sync unit, and 4fsc, HR, VR, and SC COM (LALTR and H COM (PAL only)) pulses are input.

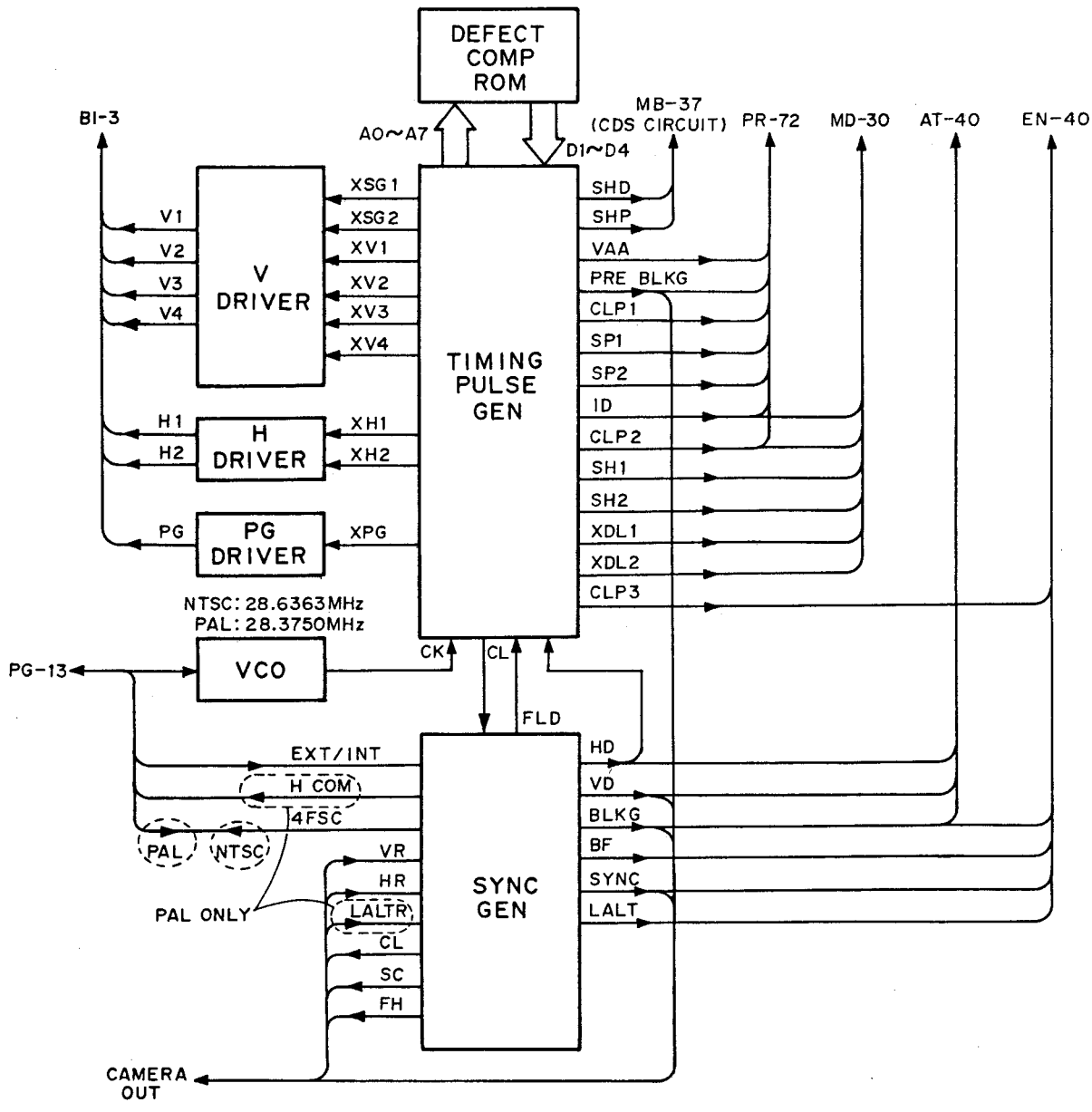


Fig. 10-1-1 PG-12 Board Block Diagram

10-2. Block Description

. Timing pulse generator (CX23047B)

When the timing pulse generator is combined with a sync generator, a pulse necessary for CCD driving and signal processing is generated. The VCO output which is generated by the DC voltage from pin 21 on the RG-13 board is used as a clock. The frequency is 28.6363MHz (1820 times the horizontal sync frequency). (For PAL, it is 28.3750MHz which is 1816 times as high.)

The clock is frequency-divided into 14.3182MHz and output as a sync generator clock. Moreover, when the HD and FLD pulses are input, the timing pulse generator is synchronized with the sync generator.

Pin No.	Name	I/O	Description
1	SP1	O	Sample & hold pulse for color separation. Provided with a defect correcting function.
2	SHD	O	Sample & hold pulse for imager output. Provided with a defect correcting function.
3	SHP	O	Pulse for sampling and holding the imager output precharge level.
4, 5 8, 9	XV1 - XV4	O	Imager driving pulse. Used as a vertical register transfer clock.
10, 11	XSG1, XSG2	O	Sensor gate 1 and 2 pulse
12	XPG	O	Precharge gate. Precharge pulse input to imager.
13, 14	XH1, XH2	O	Used as an imager driving pulse and horizontal register transfer clock.
15 - 18 20 - 22	A0 - A6		External ROM address output
19, 43	VDD	I	+5V power supply terminal
23	CM	I	Test terminal. GND
24 - 27	D4 - D1	I	External ROM input terminal
28	XVCT	O	ROM power supply switching pulse
29	TEST	I	Test terminal. GND
30	CP	I	Clock input. NTSC: 28.63636MHz
6, 31	VSS	I	GND terminal
32	XCK	O	Inverter circuit.
33	CK	I	Used for waveform shaping.

Mode setting

Pin / Value	D4	D3	D2	D1
1	NTSC	Always 1	Color	External ROM provided
0	CCIR			

Pin No.	Name	I/O	Description
34	FLD	I	Frame sync signal input. Used to distinguish odd and even fields. Loaded at the trailing edge of a CL pulse at pin 36. "H" in odd fields and "L" in even fields.
35	HD	I	Horizontal sync signal input. Loaded at the trailing edge of a CL pulse at pin 36.
36	CL	O	Sync generator (CX7930) clock output. Frequency of half a CP pulse.
37	VAA	O	Vertical effective area of CCD imager output (vertical preblanking). Used together with a CLP1 pulse in clamp circuit. The VAA output is phase-inverted using Q1, Q2, and Q3 and input to the CB, CR, and CG terminals of pins 34, 35, and 36 of CX20053.
38	H BLK	O	Horizontal preblanking of CCD imager output. Input to pin 38 of CX20053.
39	ID	O	Linear sequential discriminating signal. "H" in line B and "L" in line R.
40	CLP3	O	Clamp pulse. Continuous pulse. . Sent to an encoder at pin 4 of CX20055.
41	CLP2	O	Clamp pulse. Continuous pulse. . Sent to a matrix at pin 17 of CX20151. . Sent to a 1H-delay line at pin 1 of CX23039.
42	CLP1	O	Clamp pulse. Clamp pulse at CCD output optical black level. . Sent to a process circuit at pin 40 of CX20053. . Sent to an auto IC at pin 1 of CX20056.
44	XDL2	O	CCD DL driving pulse (1H-delay line CX23039 driving)
45	XDL1	O	CCD DL driving pulse (1H-delay line CX23039 driving)
46	SH2	O	CCD DL driving pulse (sample & hold pulse for 1H-delay line CX23039)
47	SH1	O	CCD DL driving pulse (sample & hold pulse for 1H-delay line CX23039)
48	SP2	O	Sample & hold pulse for color separation. Provided with a defect correcting function.

. Defect correcting ROM (1024-bit) (MB7052)

Defective CCD data is input to the ROM. ADRS is dertermined by addresses A0 through A6 of CX23047B. When defects are found in the CCD, CX23047B loads data D1 through D4, then is activated so that SP1, SP2, and SHD pulses are not output at this point.

. Sync generator CX7930

The output of TV sync signal generator LS1 is synchronized with the 910fH (NTSC) or 908fH (PAL) clock pulse, so it has a high-precision output pulse width.

Pin No.	I/O	Name	Description
1	IN	VRI	Vertical reset input
2	OUT	FLD1	First field output
3	OUT	BF/COLB	Burst flag/color blanking output
4	OUT	CSYNC	Composite sync output
5	OUT	FLD	Even/odd output
6	OUT	BLK	Composite blanking output
7	OUT	LALT	Line selection output (PAL)
8	OUT	HD	Horizontal drive output
9	OUT	4fscOUT	4fsc output
10	IN	4fscIN	4fsc input
11	-	NC	
12	OUT	VD	Vertical drive output
13	-	NC	
14		VSS	GND terminal
15	IN	LALTRI	Line selection reset input
16	IN	TEST	Test input (Not used)
17	-	NC	
18	-	NC	
19	OUT	OSC	Subcarrier output
20	IN	EXT	Internal/external mode selection
21	IN	MODE1	System selection input 1
22	IN	MODE2	System selection input 2
23	IN	HRI	Horizontal reset input
24	OUT	HCOMOUT	Phase comparator output (PAL)
25	OUT	CLOUT	Clock output
26	IN	CLIN	Clock input
27	OUT	OFH	Horizontal frequency output
28		VDD	Power supply terminal

Mode selection

Mode 1	Mode 2	System
0	0	NTSC
0	1	SECAM
1	0	PALM
1	1	PAL

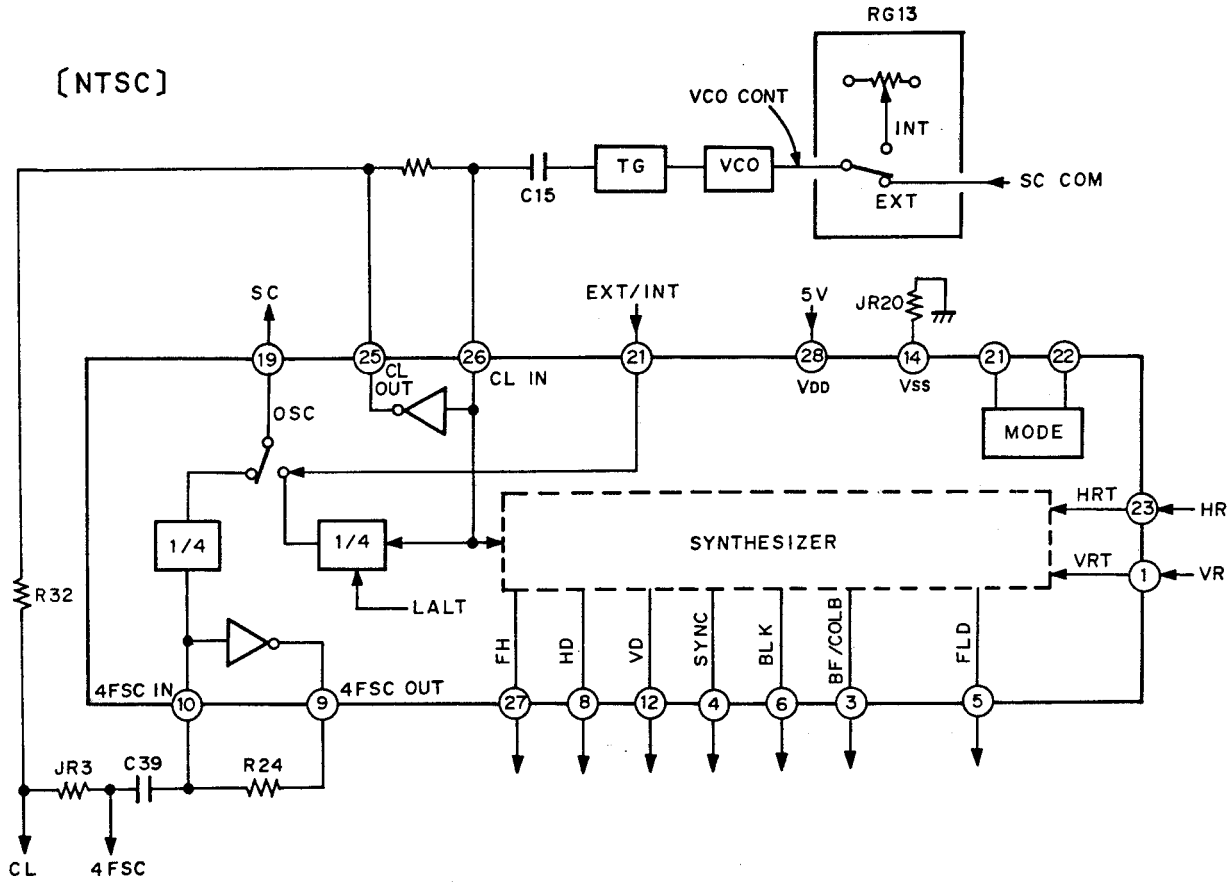


Fig. 10-2-1 CX7930 Block Diagram

A 14.3182MHz clock signal from a timing generator is input to pin 26, and each sync signal is output in synchronization with the clock pulse. For output timing, refer to the timing chart. The resultant clock pulse is output from the camera through a buffer for GEN-LOCK purposes. In the internal sync mode, the pulse is sent through the RG-13 board to the EN-40 board as a chroma signal modulation pulse (4fsc). The synthesizer is reset using horizontal and vertical driving pulses during GEN-LOCK operation.

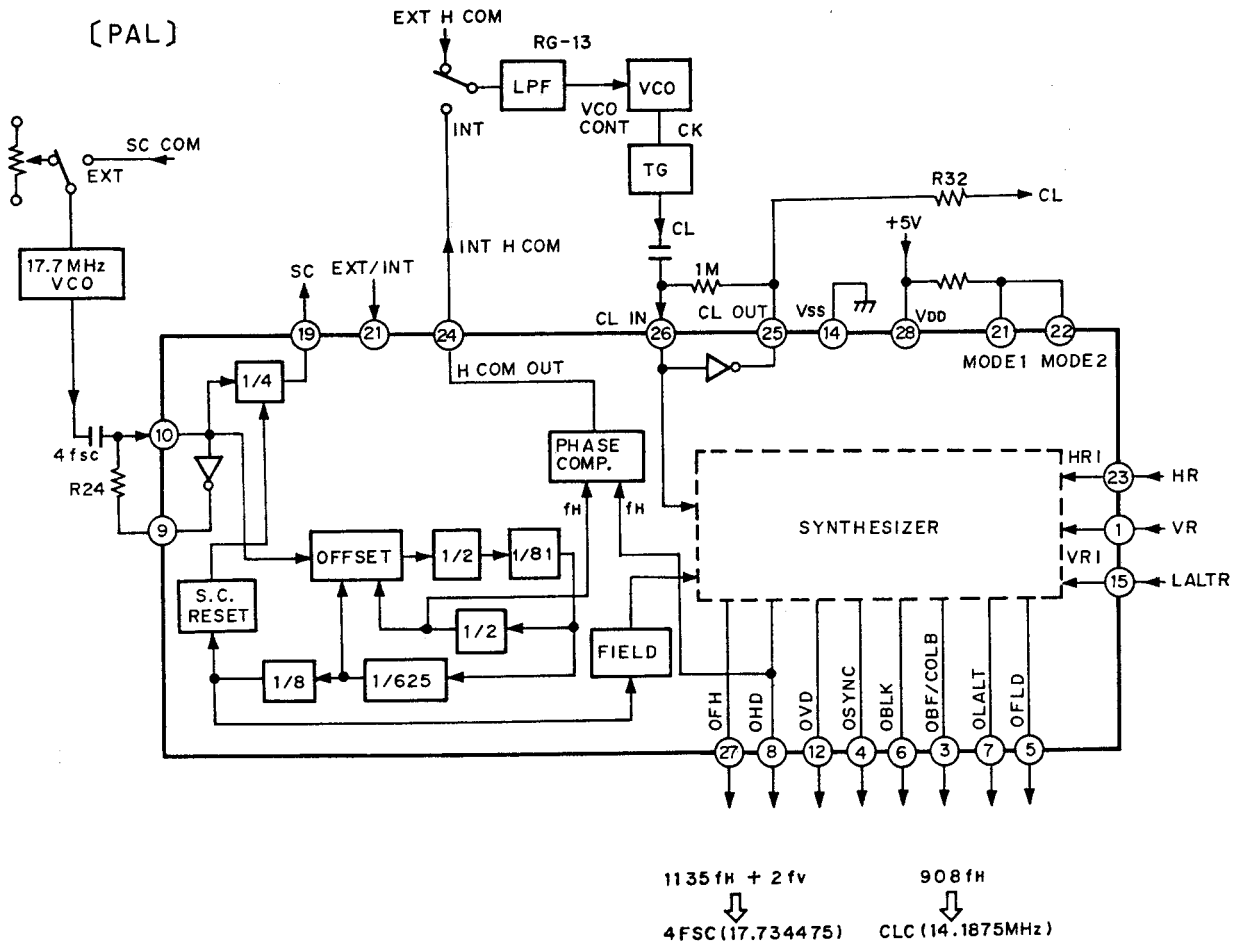


Fig. 10-2-2

For the PAL system, the clock frequency does not coincide with the 4fsc pulse frequency. Therefore, a PLL is formed to adjust the clock frequency. The 4fsc pulse is produced by the VCO on the RG-13 board.

10-3. CCD Vertical Driver CX20180

The CX20180 is a capacitor load drive IC of large capacitance and is used to drive CCD vertical clock driving. It has the following features.

(1) Four independent CCD drive blocks

(2) Readout pulse inverter block

(3) Negative voltage generator block

(4) Blanking block to reduce power consumption

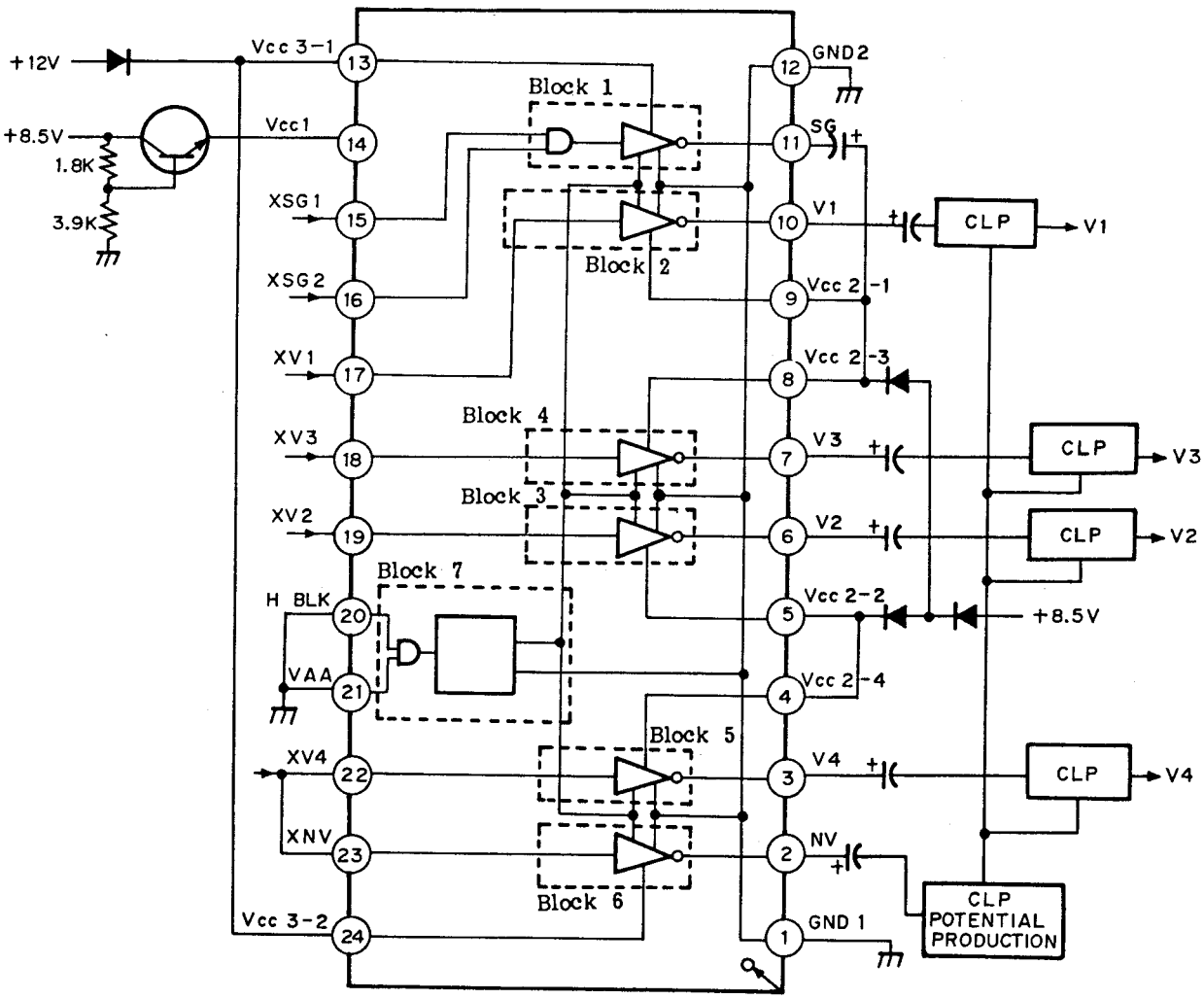


Fig. 10-3-1 Block Diagram and Pin Assignment

The CX20180 enables a compact CCD to be driven with low power consumption. It consists of seven blocks forming a vertical clock driver.

. Block 1 (signal generator)

Block 1 is an inverter with a two-input AND gate and is used to produce a readout pulse outside an IC.

. Blocks 2 through 5

Blocks 2 through 5 are four identically configured inverters which drive an actual CCD imager. The four drive circuits have internal coupling suppressors so that they are not coupled by the junction capacitance between the CCD phases.

. Block 6

The pulse output from block 6 is sent to an external circuit, rectified, and converted into a negative voltage to clamp signals appearing at blocks 2 through 5.

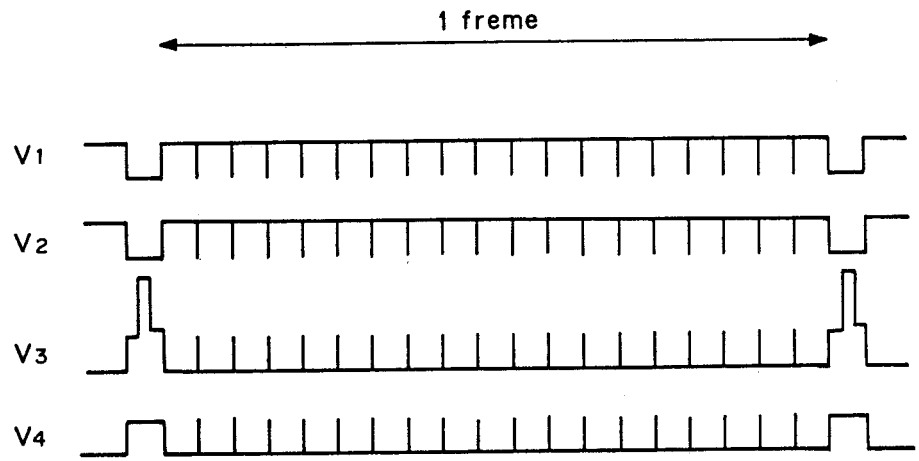


Fig. 10-3-2 Output Waveforms

10-4. CCD Horizontal Driver MMH0026

The XH1 and XH2 pulses from timing pulse generator CX23047 are inverted and voltage-converted using MMH0026 and sent to the CCD.

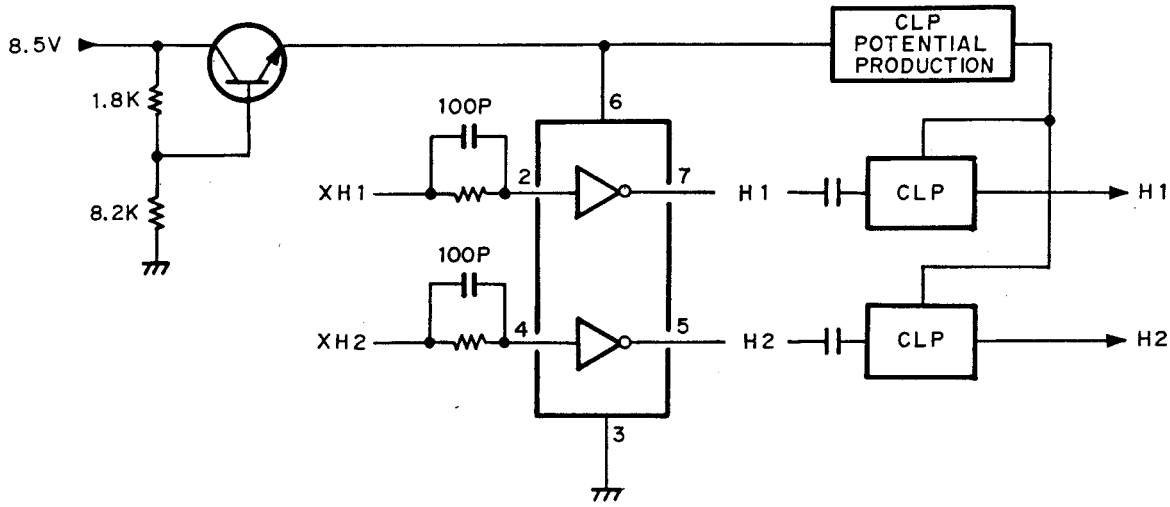


Fig. 10-4-1

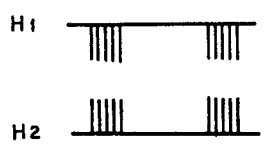


Fig. 10-4-2 Output Waveforms

PG driver

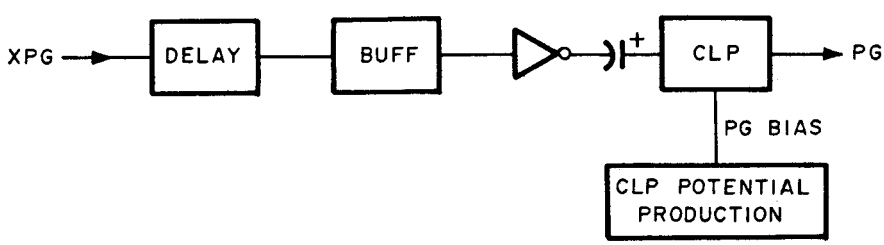
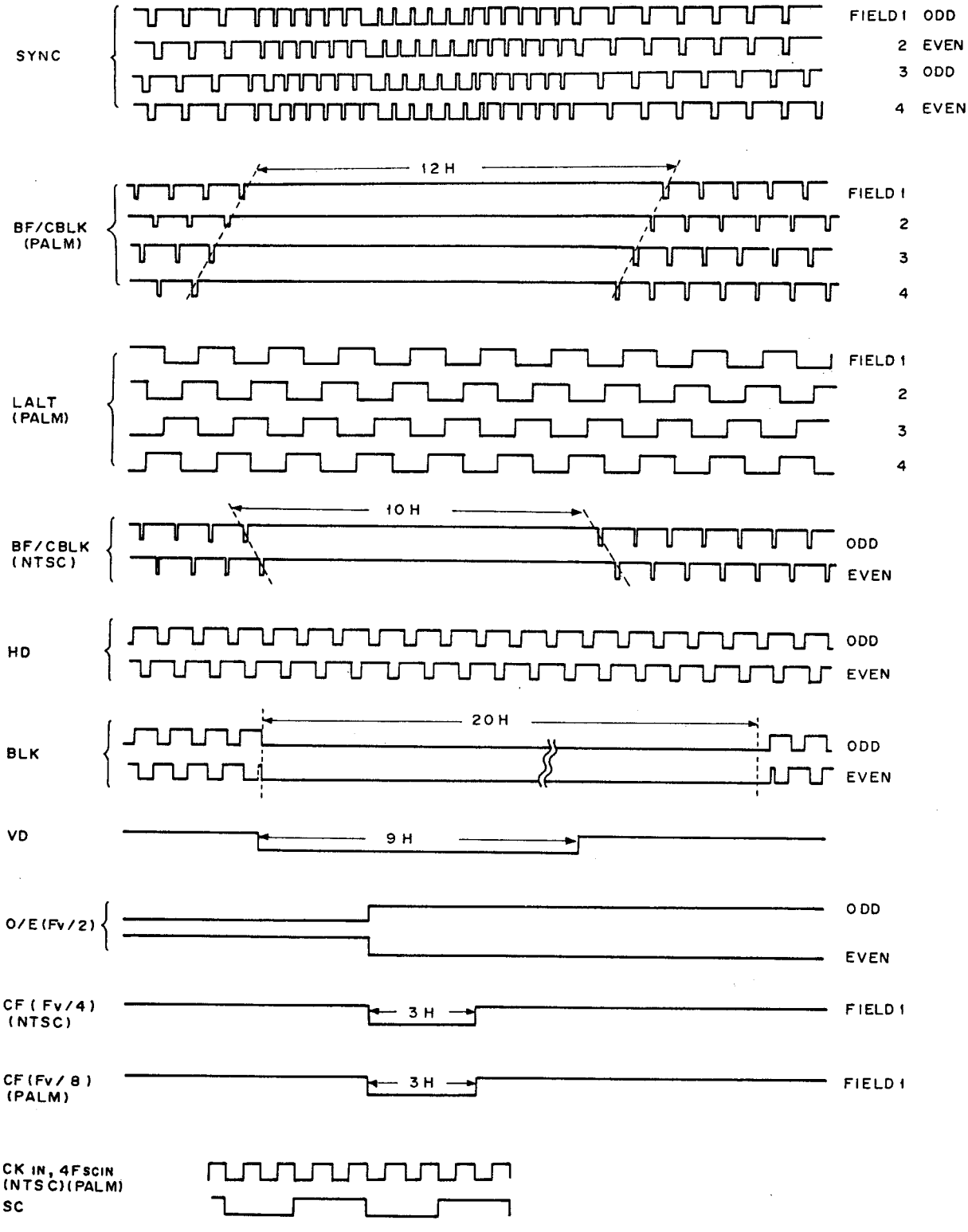
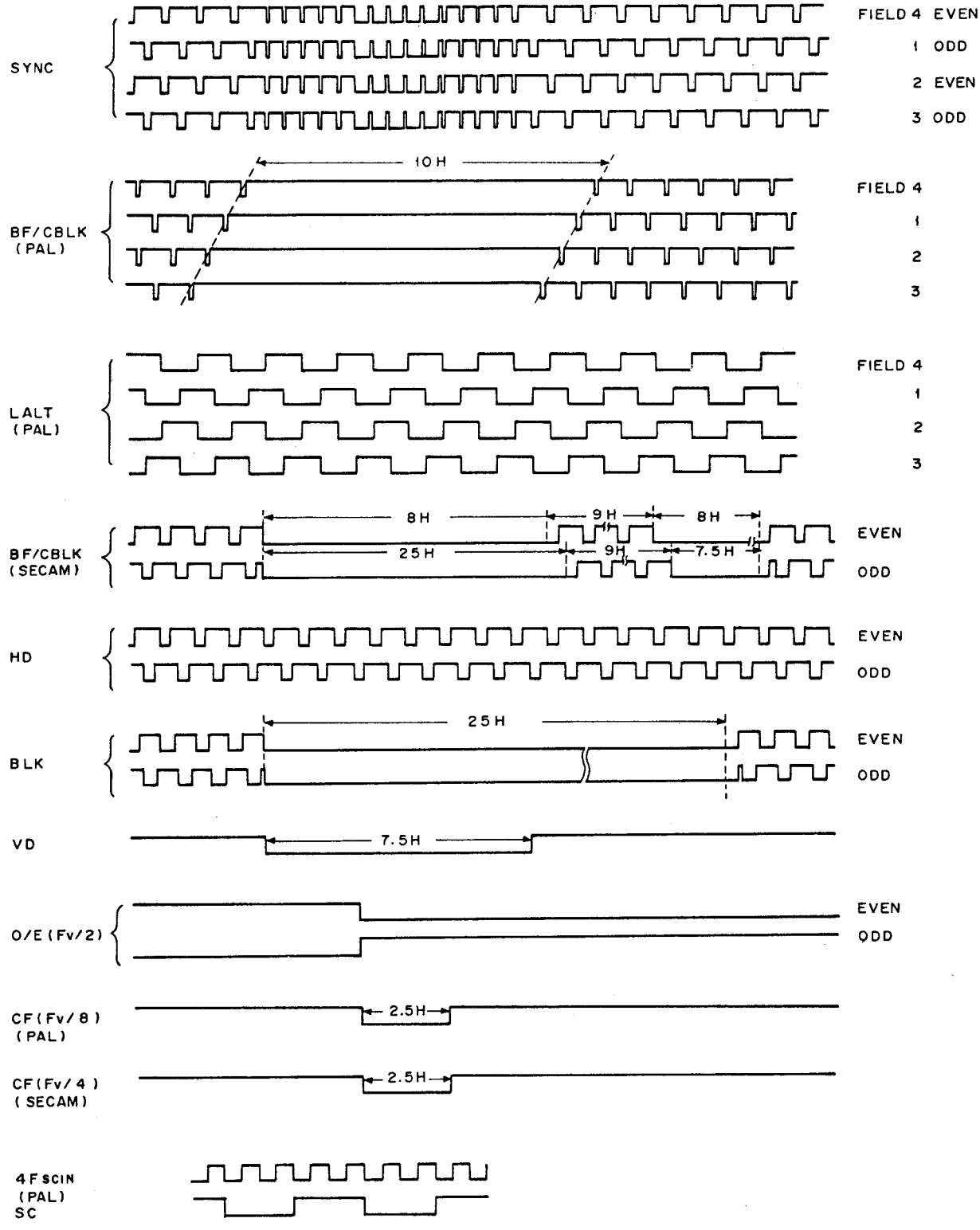


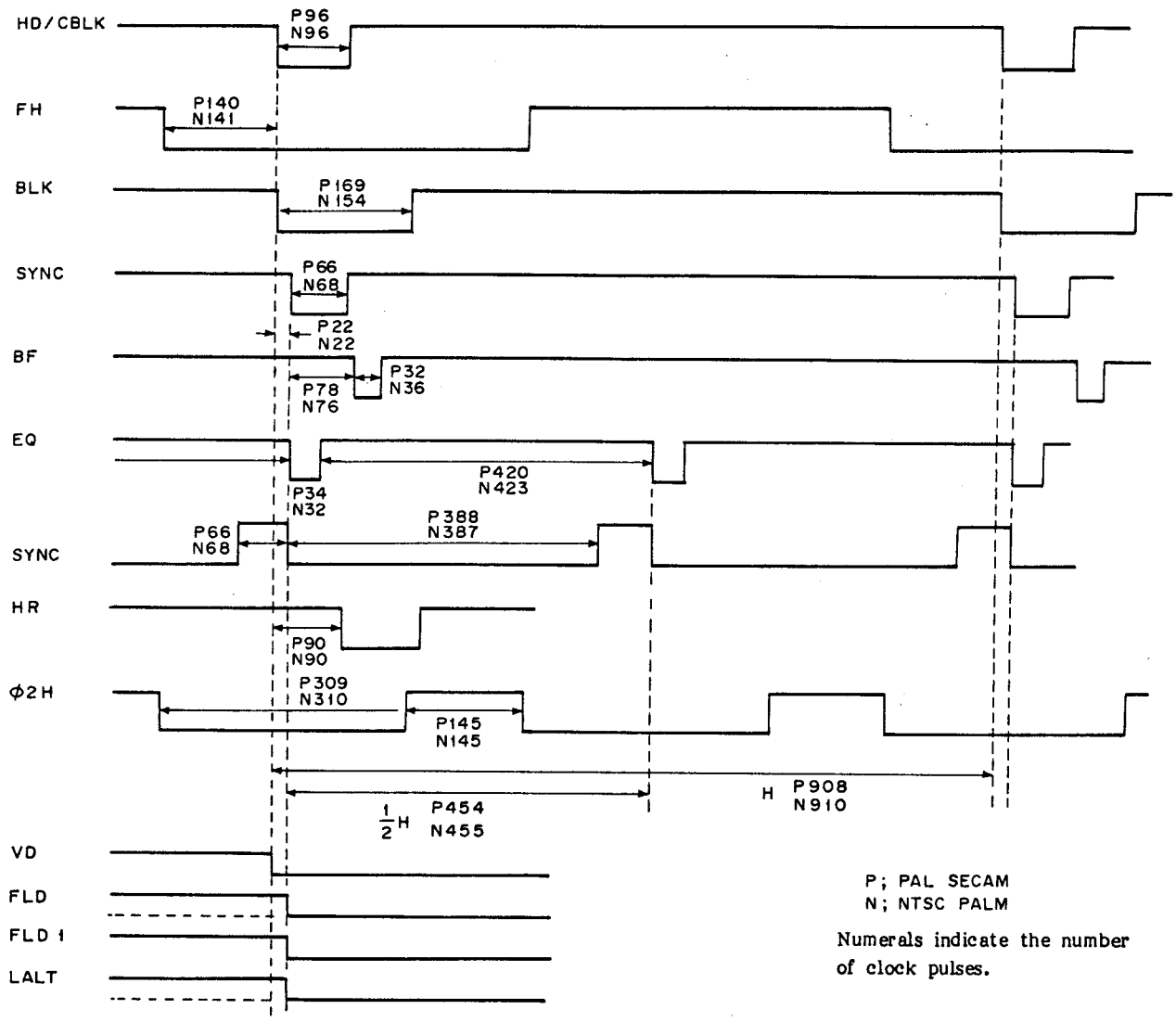
Fig. 10-4-3

The XPG pulse from the timing pulse generator is phase-adjusted, then passed through Q1 through Q4 as a CCD PG driving pulse.


SYNC
FIELD 1 ODD
2 EVEN
3 ODD
4 EVEN
12 H
BF/CBLK (PALM)
FIELD 1
2
3
4
LALT (PALM)
FIELD 1
2
3
4
10 H
BF/CBLK (NTSC)
ODD
EVEN
HD
ODD
EVEN
20 H
BLK
ODD
EVEN
VD
9 H
O/E (Fv/2)
ODD
EVEN
CF (Fv/4) (NTSC)
3 H
FIELD 1
CF (Fv/8) (PALM)
3 H
FIELD 1
CK IN, 4FSCIN (NTSC) (PALM)
SC

CX-7930A PAL, SECAM

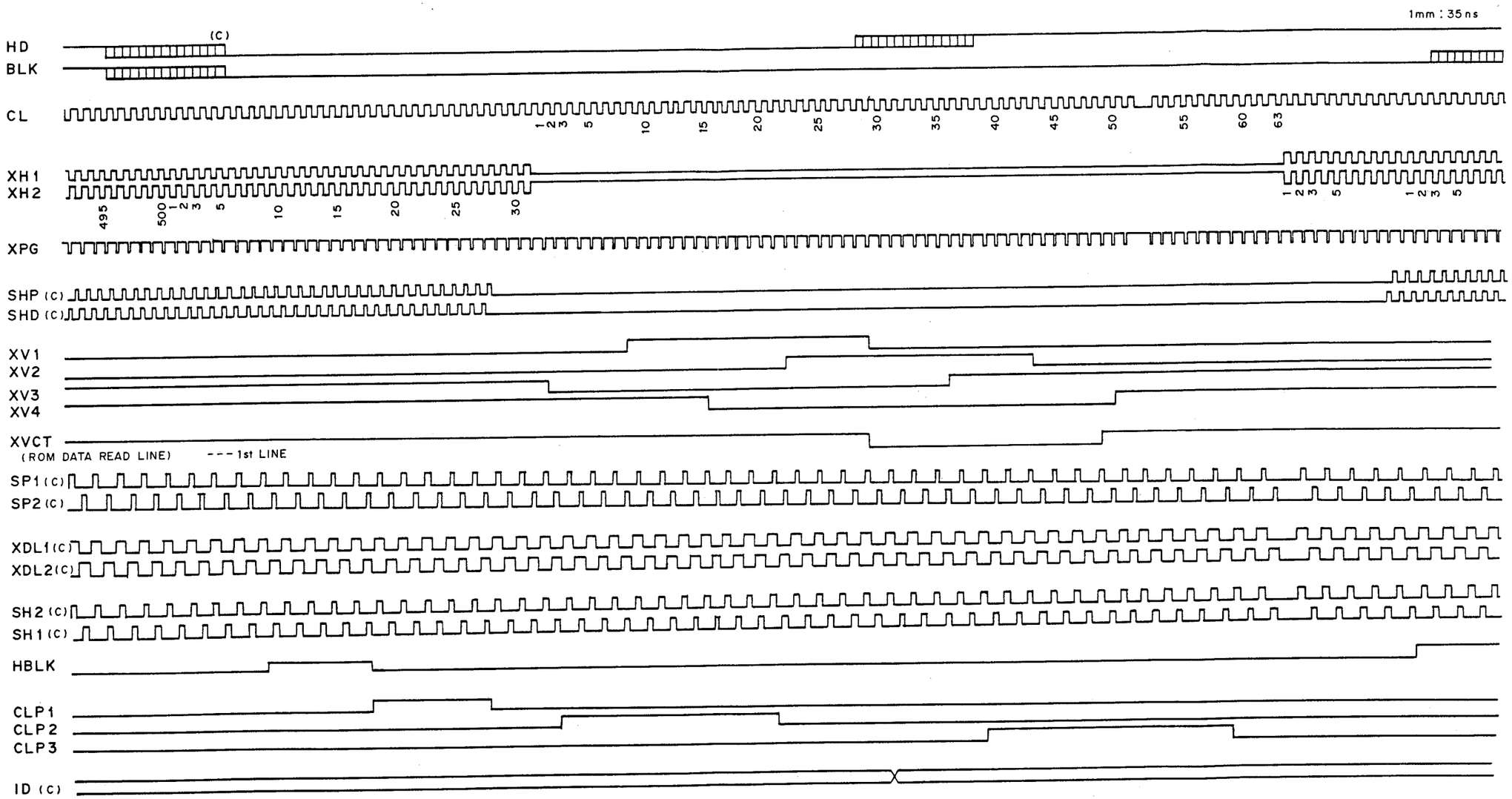




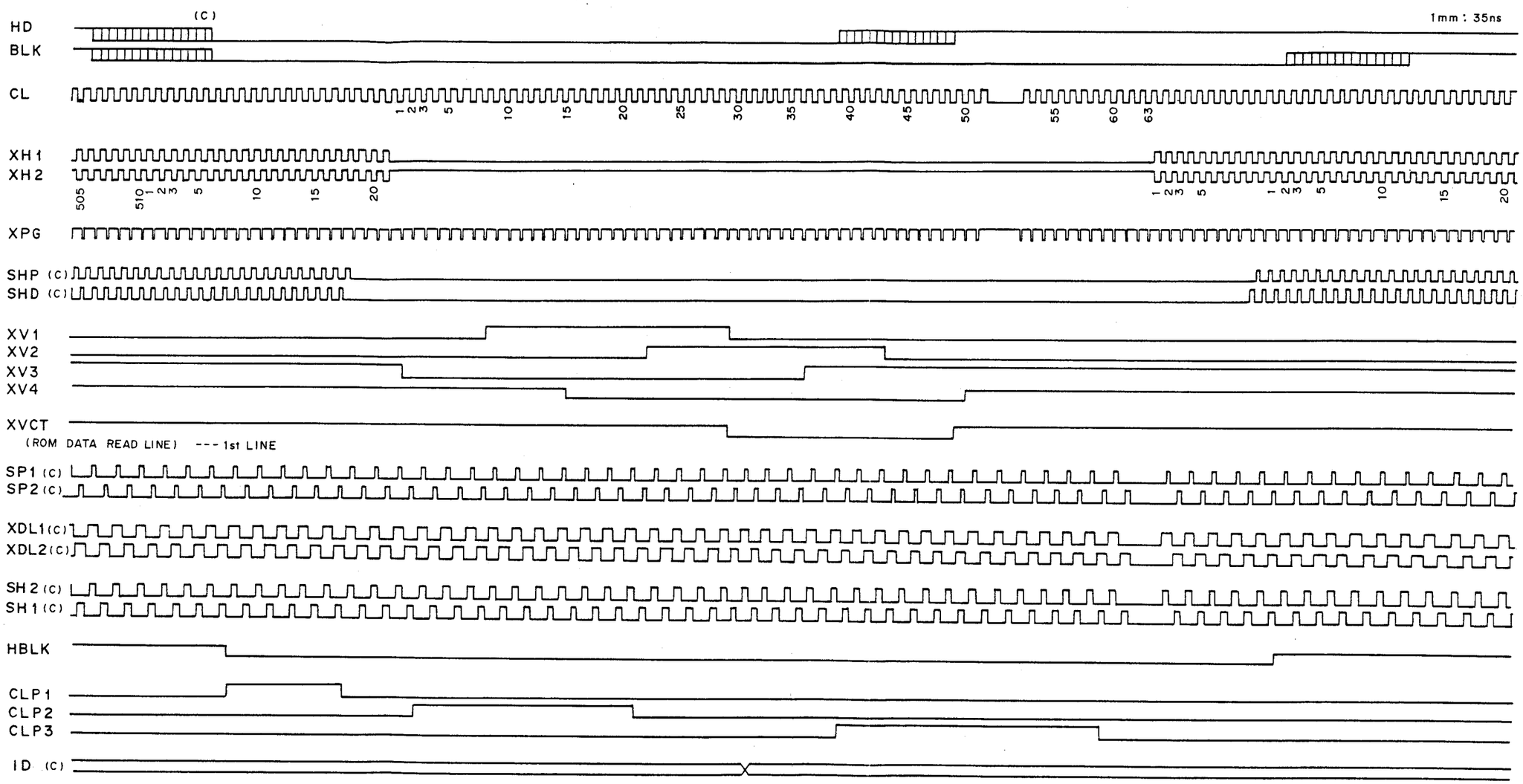
P; PAL SECAM
N; NTSC PALM

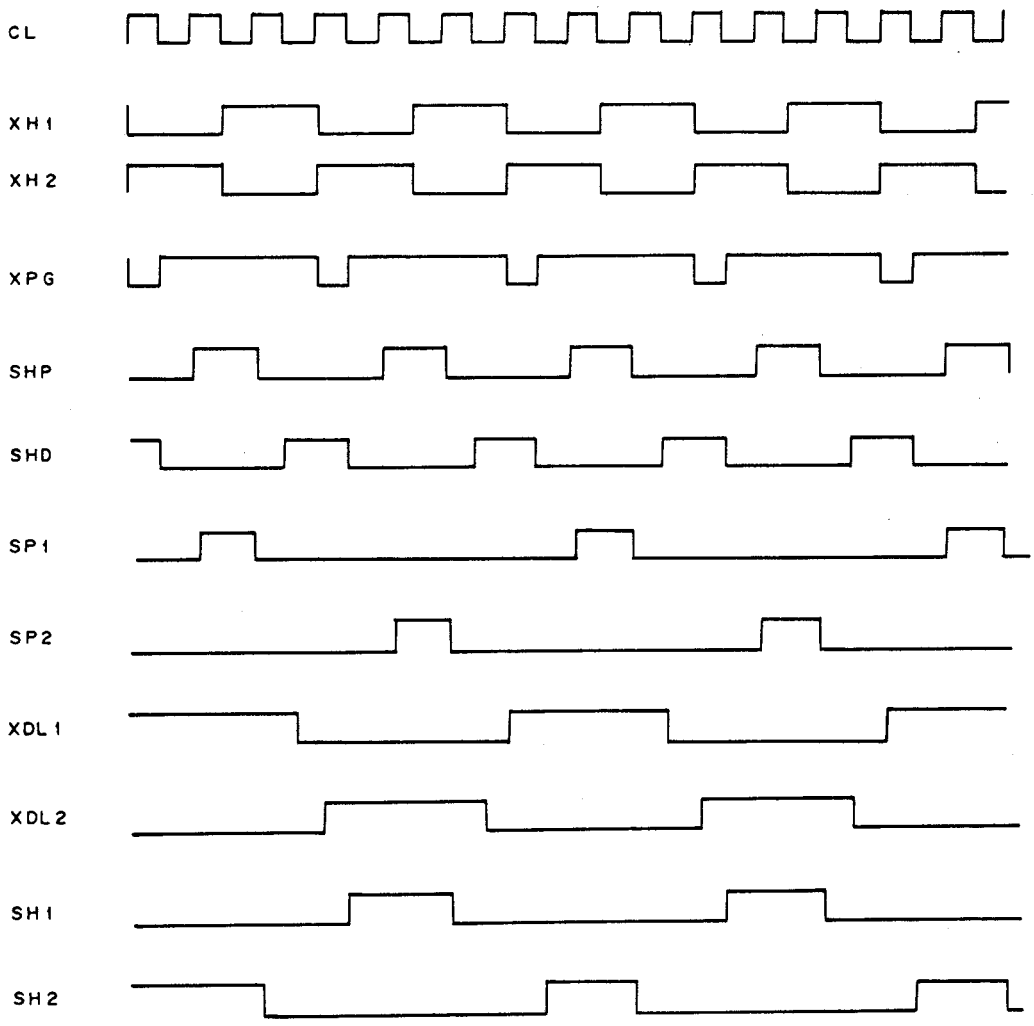
Numerals indicate the number of clock pulses.

CX23047B (CCIR) (ROM OFF)



CX23047E (NTSC) (ROM OFF)




CL
XH1
XH2
XPG
SHP
SHD
SP1
SP2
XDL1
XDL2
SH1
SH2

11. CONNECTOR BOARD CN-116

11-1. Outline

When a 50-pin connector on the camera is connected to a 50-pin connector on the CN-116 board, the white balance gain can be set.

11-2. White Balance Setting

The white balance adjustment has four modes, which are determined by pins 7 and 8 as follows:

	AUTO	3200° K	Outdoors	Indoors
WB CONT 1 pin 7	H	L	H	L
WB CONT 2 pin 8	H	L	L	H

- The high signal becomes +5V when it is used outside of this board.
- The low signal is connected to GND when it is used outside of this board.

When the signals at pins 2 and 8 go high, the unit enters the AUTO white mode, Q4 is turned on, the base of Q5 goes high, and the signal at pin 3 of IC1 (1/2) goes high. An AWB TRIG pulse from pin 3 can then be loaded. For the AWB TRIG pulse, when pin 3 is connected to GND, Q1 is turned on, the signal at pin 4 of IC1 (1/2) goes high, and IC1 (1/2) is set using the rising pulse. The truth table of IC1 is shown below.

Truth table

Input			Output		NOTE
A	B	CD	Q	$\overline{Q}$	
↓	H	H	⊓	⊔	OUTPUT ENABLE
↓	L	H	L	H	INHIBIT
H	↑	H	L	H	INHIBIT
L	↑	H	⊓	⊔	OUTPUT ENABLE
*	*	L	L	H	INHIBIT

* Don't Care

The Q output pulse width of IC1 pin 6 is determined by the time constant of R1 and C1 (approximately 0.4sec). The high pulse is input to the AT-40 board as an AWB TRIG pulse. The resultant output pulse turns on Q3, makes the base of Q2 high, inhibiting the AWB indicator operation.

When power is turned on, Q6 inhibits the auto white balance operation for a while and is turned on for an interval determined by the time constant of R9 and C7. The collector of Q5 then goes low and the INHIBIT signal at pin 3 of IC1 (1/2) remains low. At that time, the AWB TRIG pulse cannot be input.

The AWB IND signal (negative pulse) from pin 4 on the CN-116 board is output as an AUTO white indicator signal. After auto white balance adjustment is completed, the signal at pin B7 of connector CN1 goes from high to low and Q is turned off. The negative pulse at Q2 collector then makes output pin 9 of IC1 (2/2) low. The output pulse width is determined by the time constant of R8 and C3 (approximately 5 to 6sec).

11-3. Gain Control

Gain control signals are input from pins 5 and 6. Mode setting is shown below.

	AUTO	0dB	6dB	9dB
Gain 1 pin 5	H	L	H	L
Gain 2 pin 6	H	L	L	H

- The low signal is connected to GND when it is used outside of this board.
- The high signal becomes +5V when it is used outside of this board.

Connection

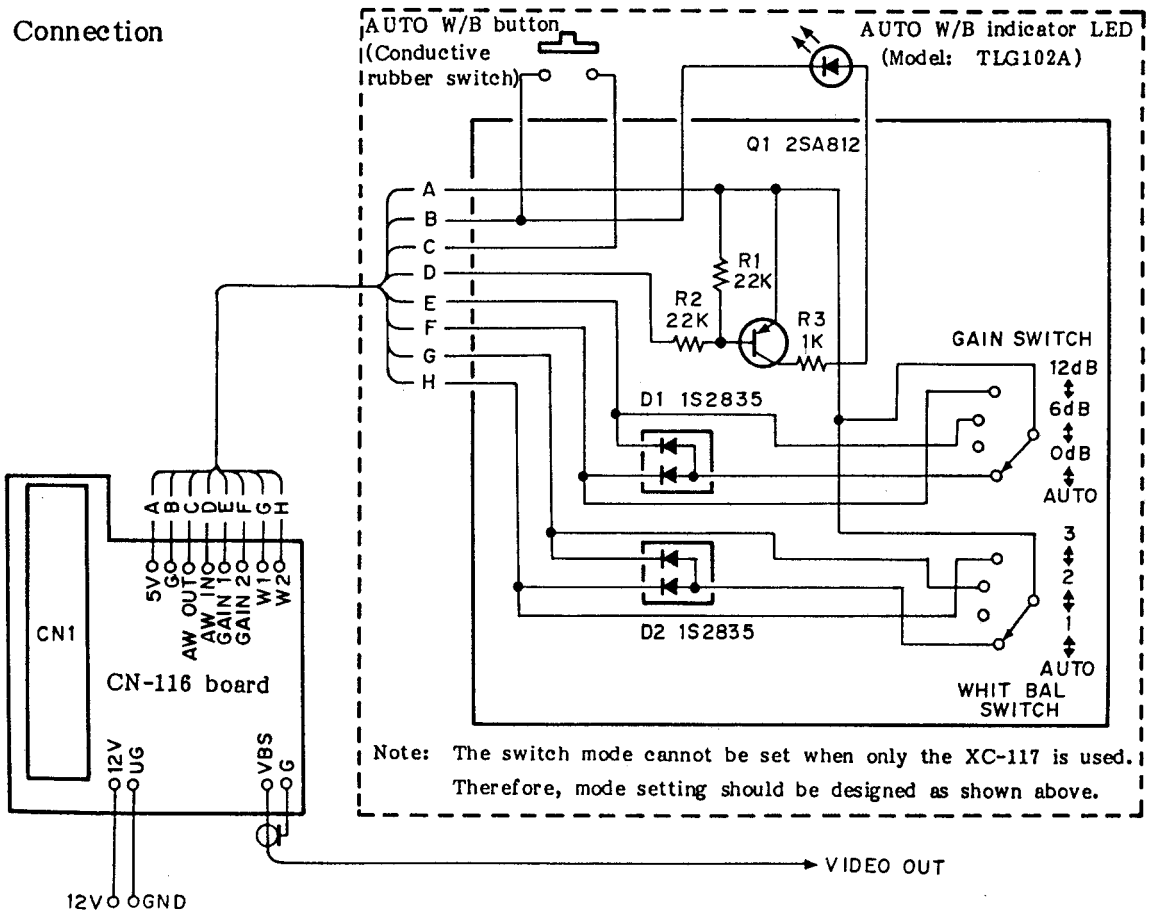


Fig. 11-3-1

12. POWER UNIT PU-1

The power unit is located in a shielded case and has an internal DC-DC converter.

An input voltage of +10.5 to +17V provides stable +20V, +8.5V, and -5V output voltages.